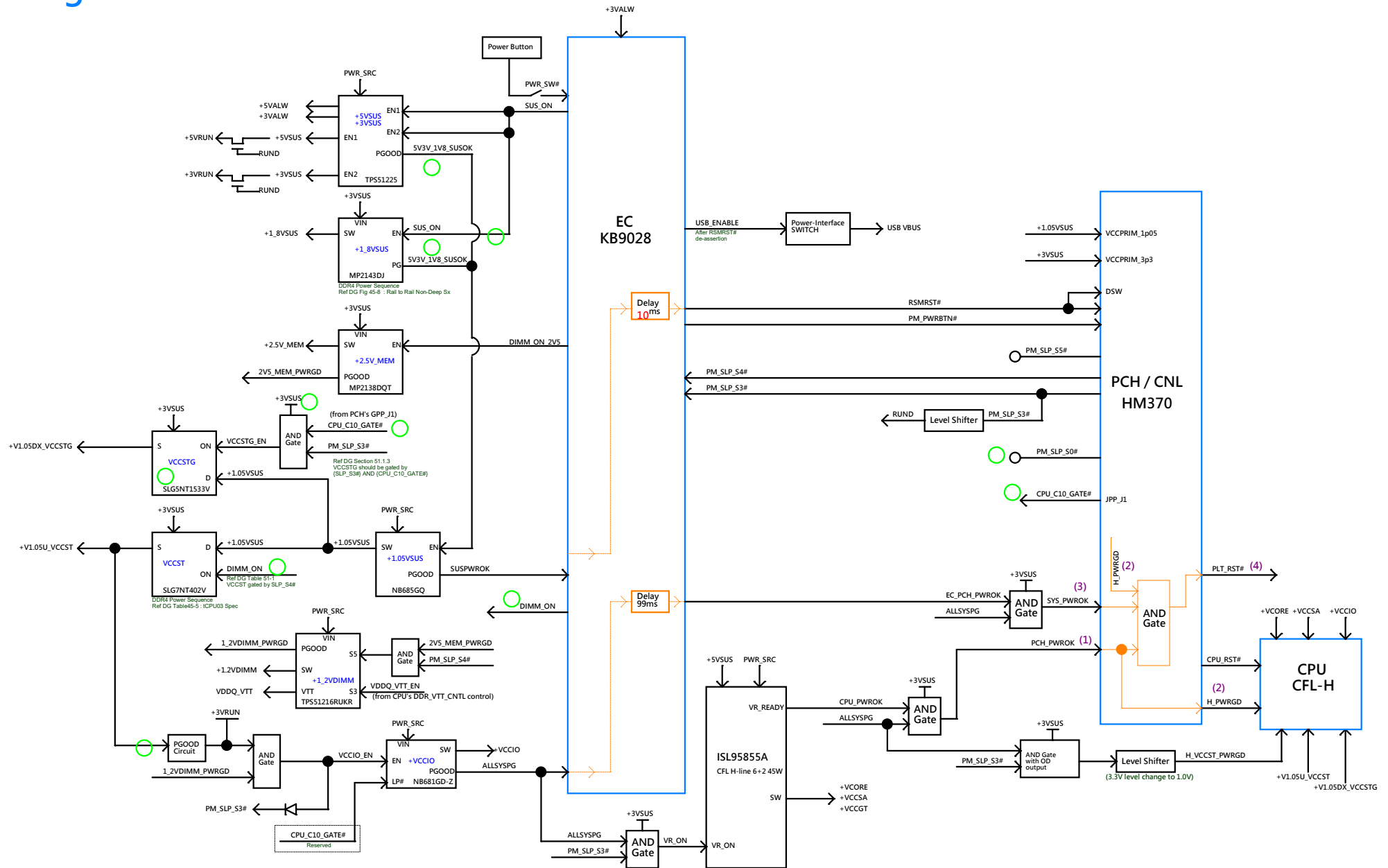
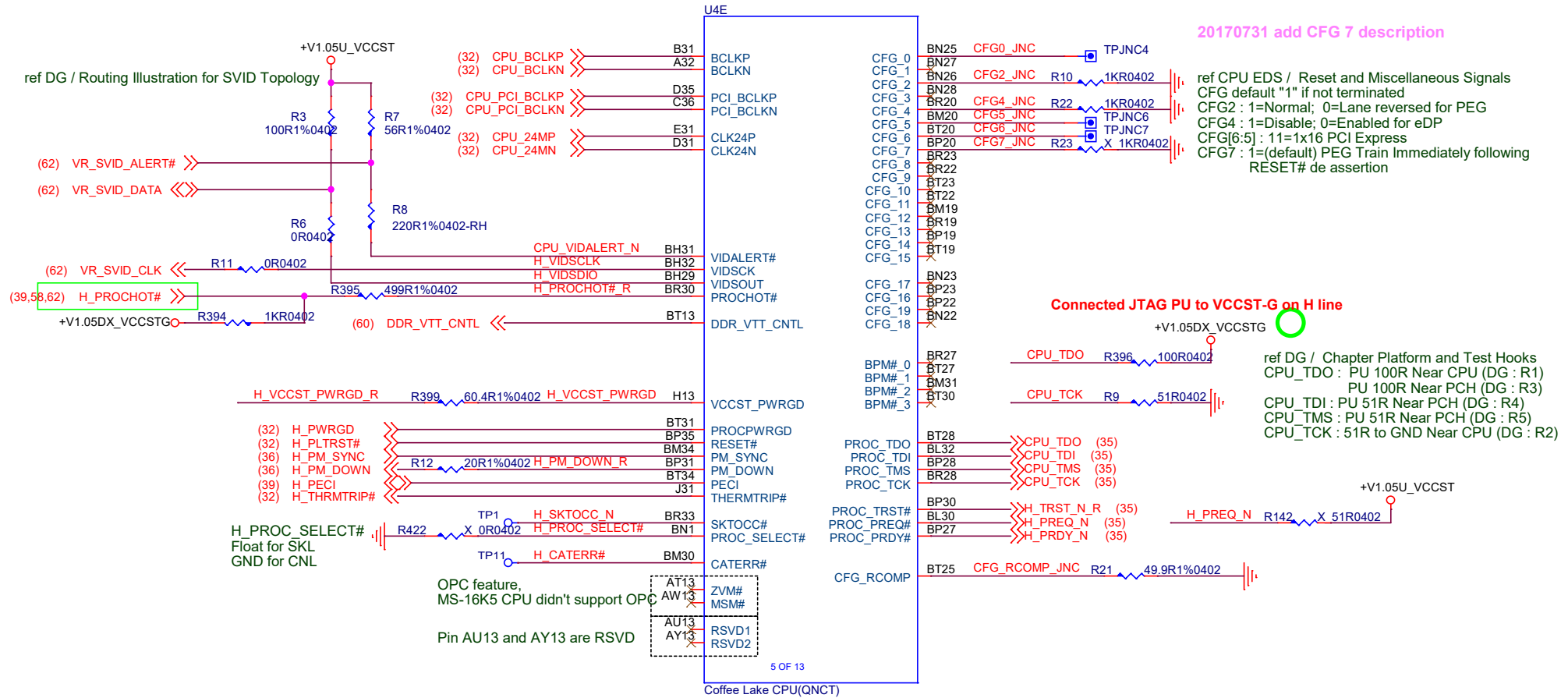


MS-16K5 : CFL-H Mobile Power on Block

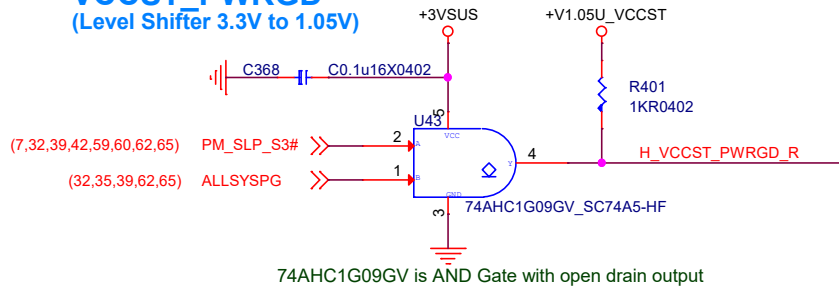
ref DG Chapter 4: Power Sequencing Spec
Diagram



CFL-H (HOST)



VCCST_PWRGD (Level Shifter 3.3V to 1.05V)



DDR Channel A

DDR Channel B

20170731 the three Resistance close CPU

msi MICRO-STAR INT'L CO.,LTD.

CFL-H(DDR4)

MS-16Q2

Thursday, January 25, 2018

Sheet 4 of 73

Rev 10

DDR Channel A

DDR Channel B

20170731 the three Resistance close CPU

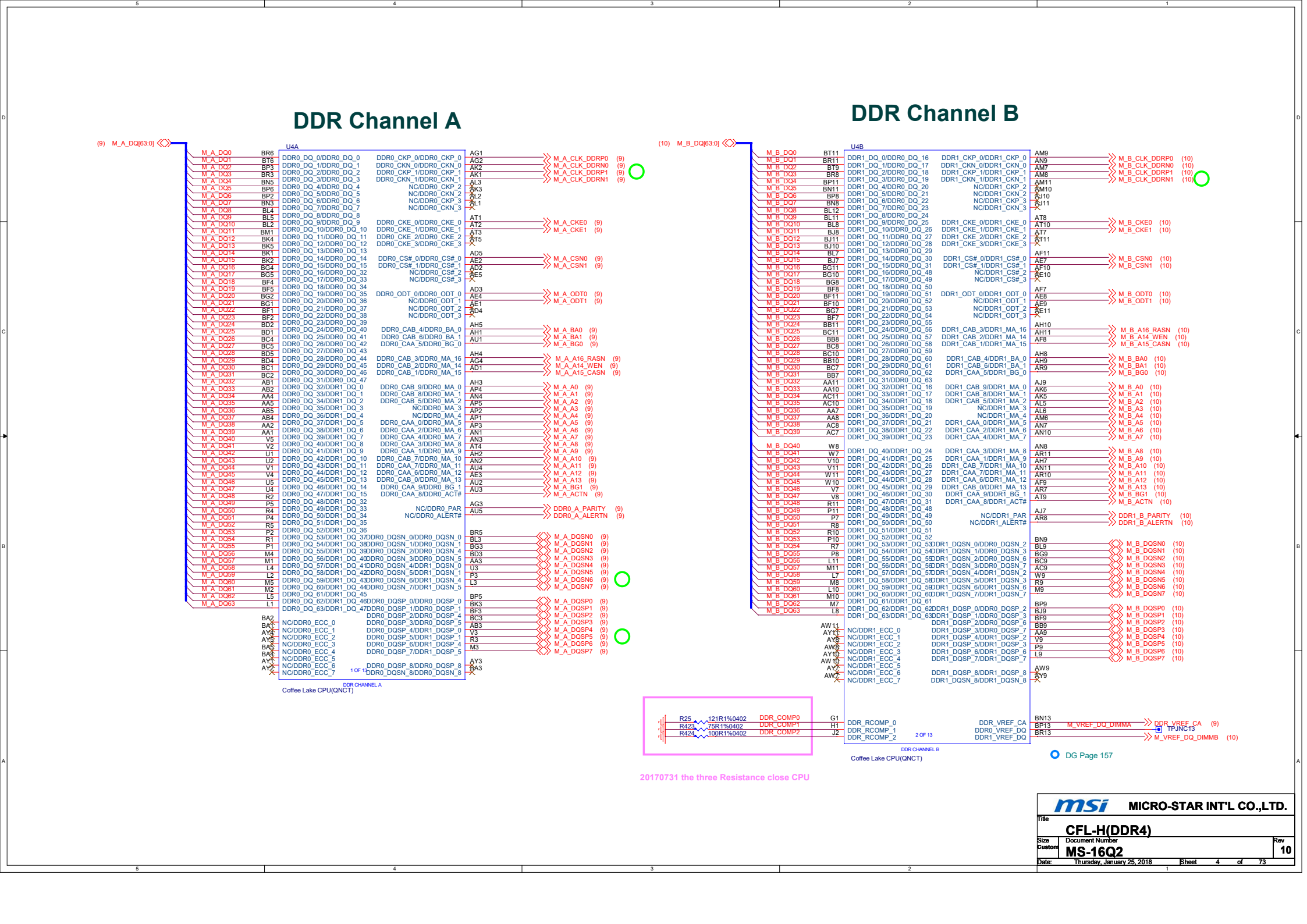
msi MICRO-STAR INT'L CO.,LTD.

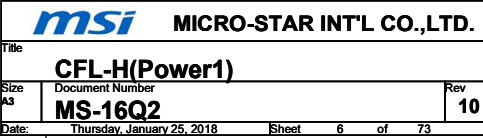
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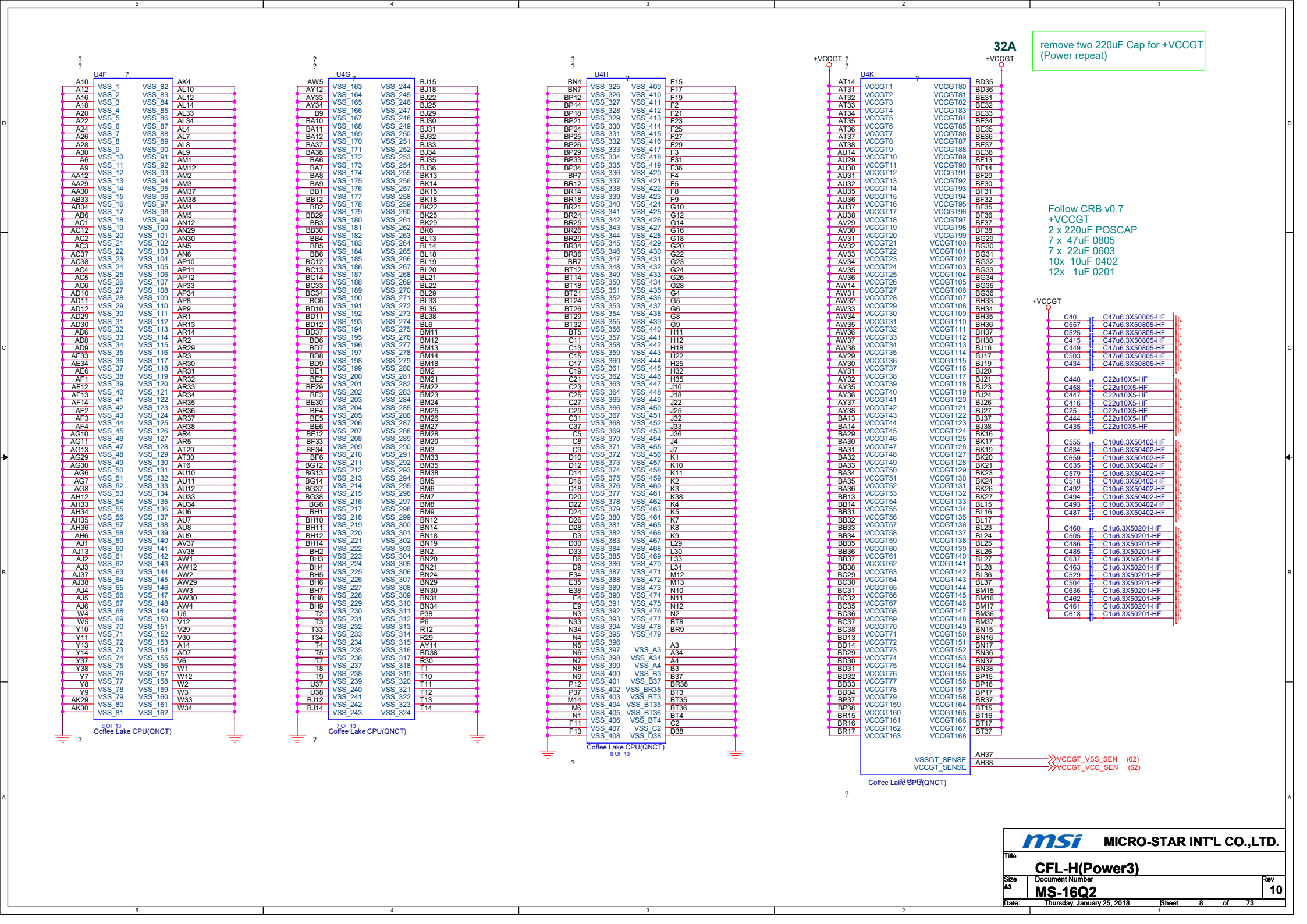
MS-16Q2

Thursday, January 25, 2018

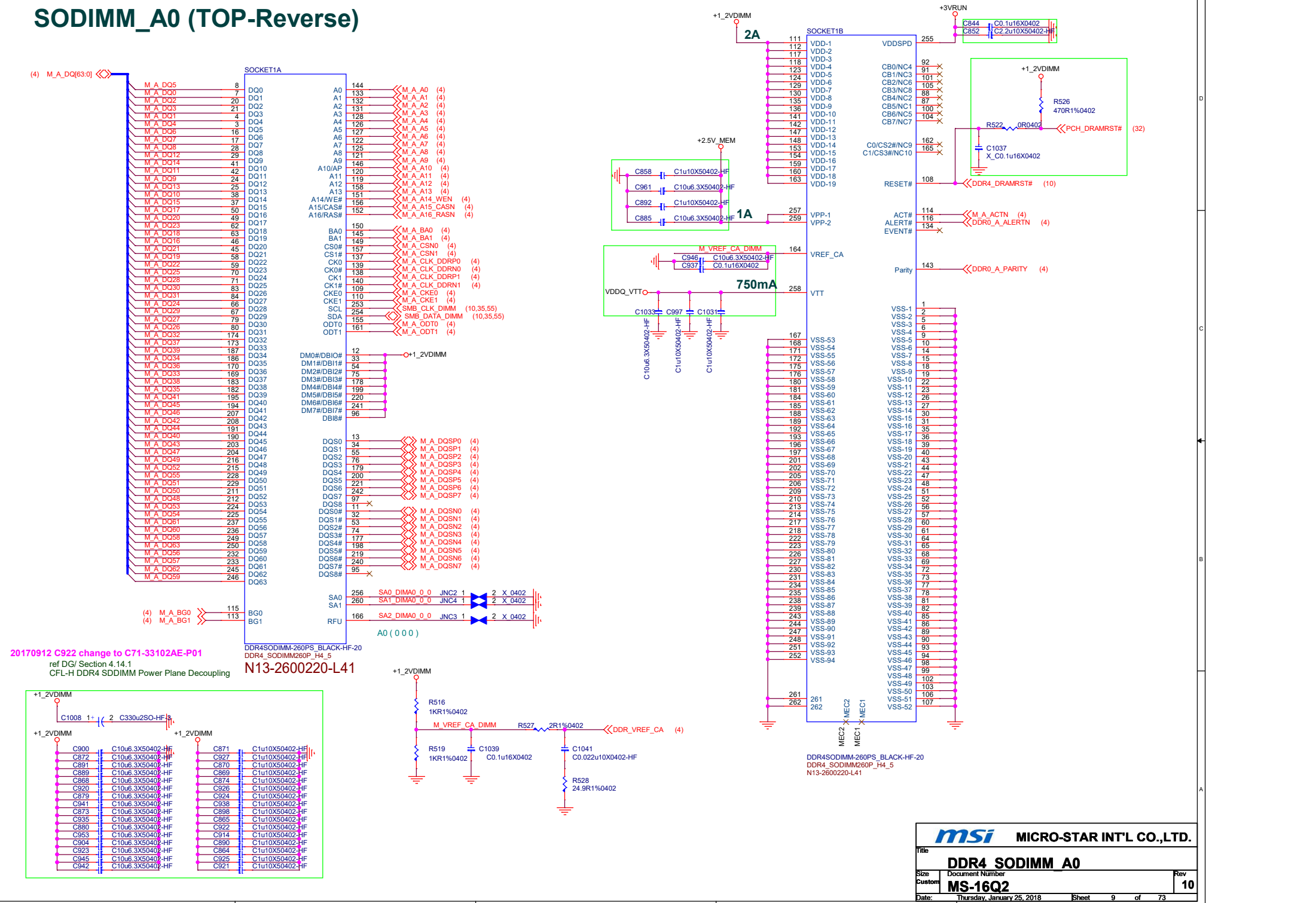
Sheet 4 of 73



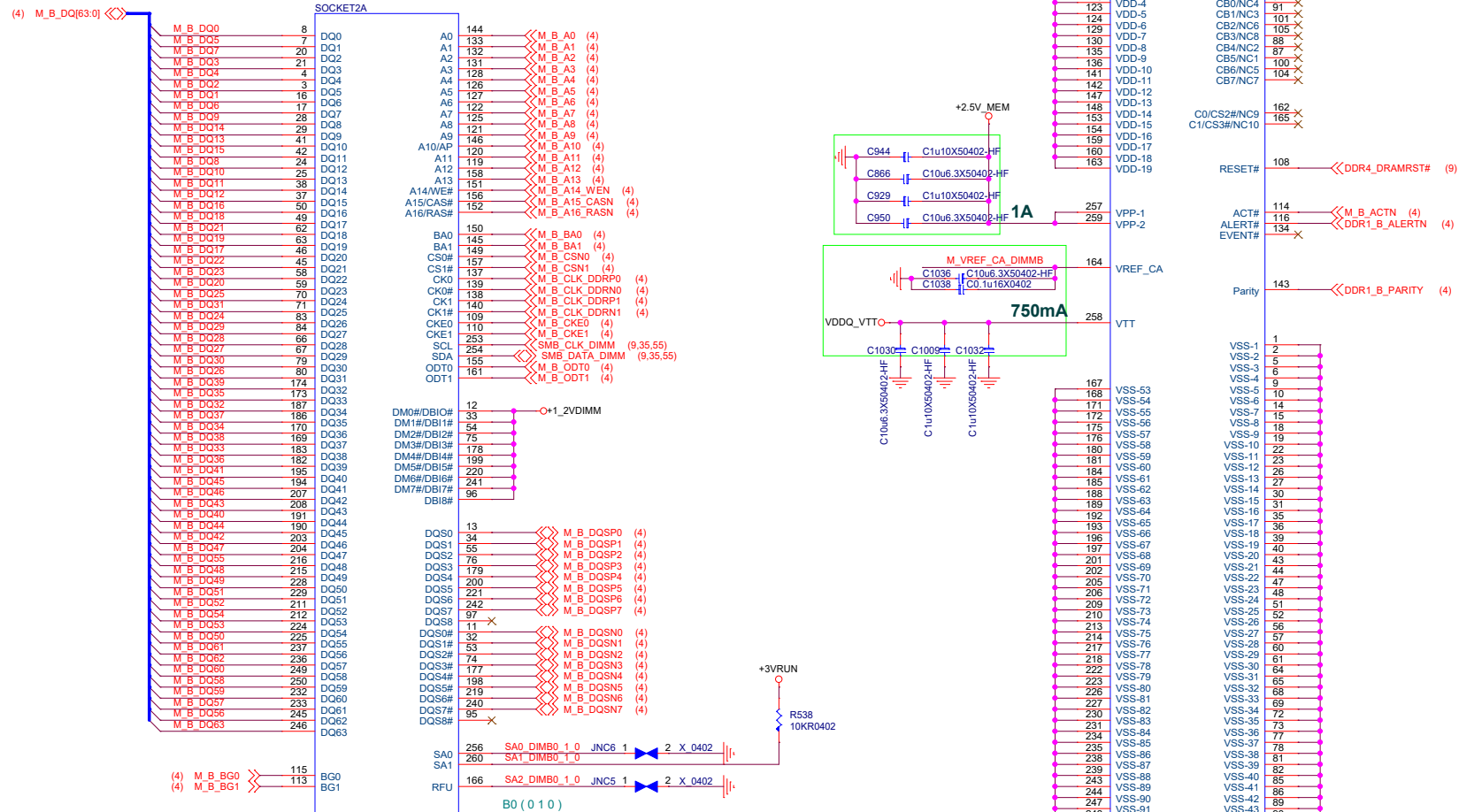




SODIMM_A0 (TOP-Reverse)



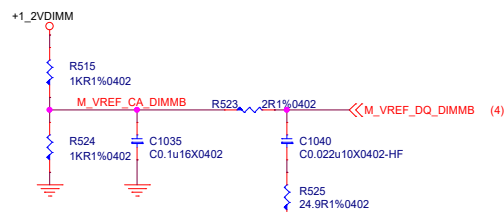
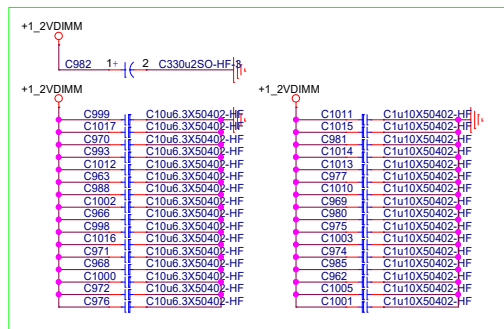
SODIMM_B0 (TOP-Standard)



DDR4SODIMM-260PS_BLACK-HF-19
DDR4_SODIMM260P_H4_3
N13-2600230-L41

20170912 C872 change to C71-33102AE-P01

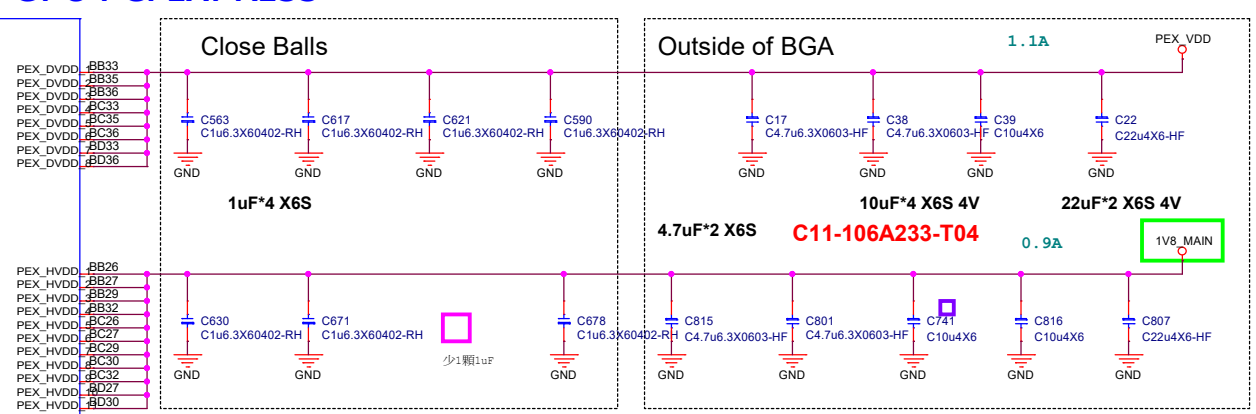
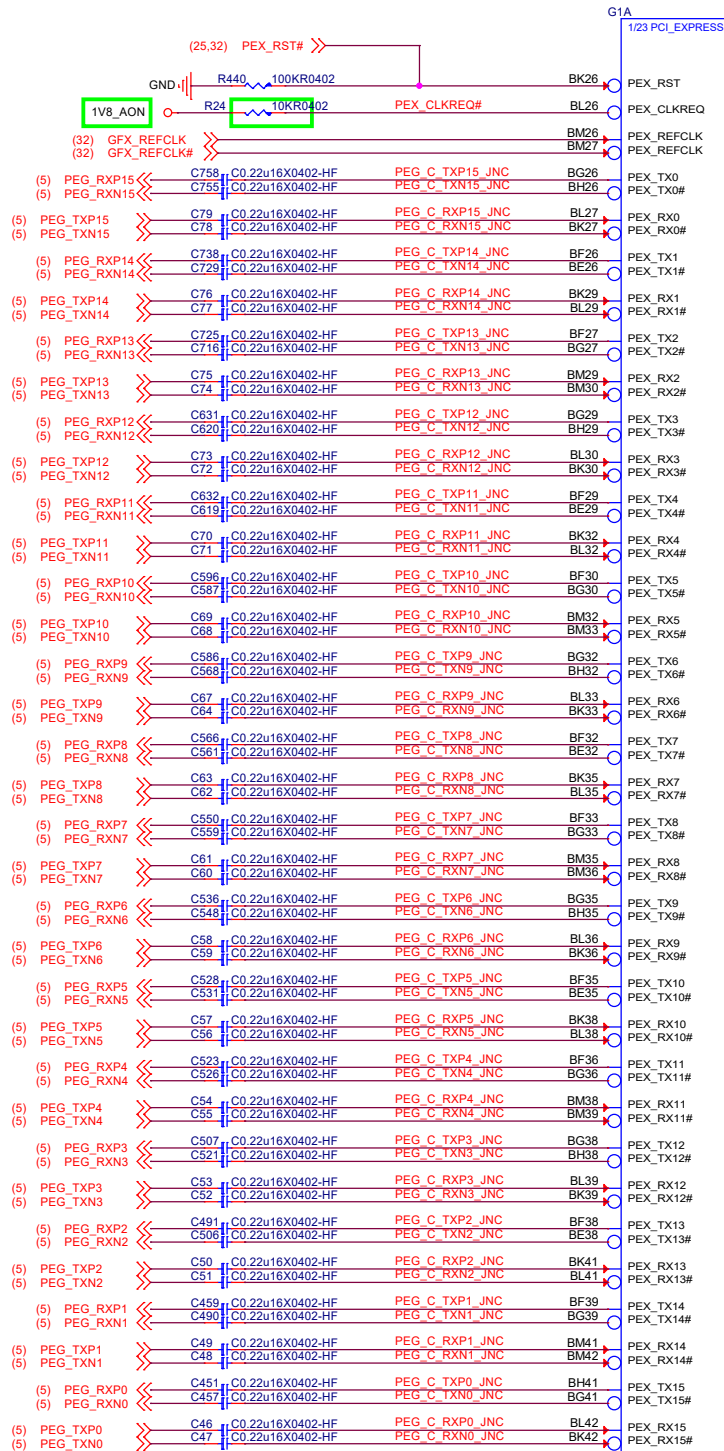
ref DG/ Section 4.14.1
CFL-H DDR4 SDDIMM Power Plane Decoupling



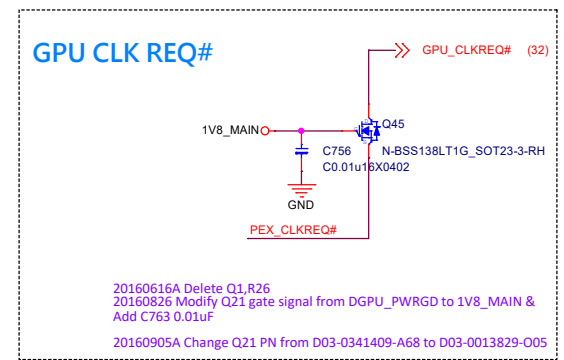
DDR4SODIMM-260PS_BLACK-HF-19
DDR4_SODIMM260P_H4_3
N13-2600230-L41

 MICRO-STAR INT'L CO.,LTD.	
Title	
DDR4 SODIMM_B0	
Size	Document Number
Custom	MS-16Q2
Date:	Thursday, January 25, 2018
Sheet	10 of 73
Rev	10

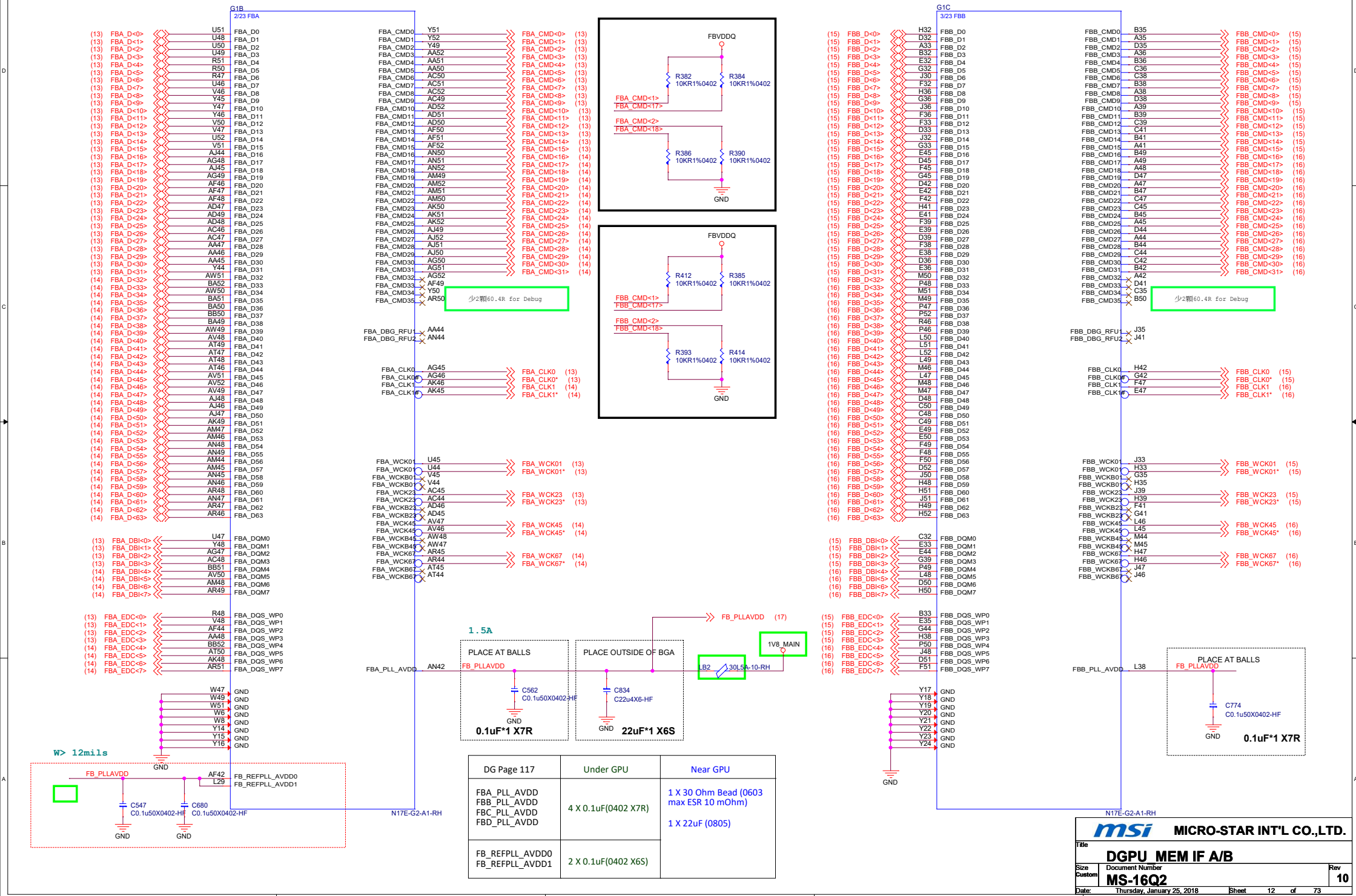
GPU PCI EXPRESS



DG Page 117	Under GPU	Near GPU
PEX_HVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 1 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	1 X 0.1uF(0402)	

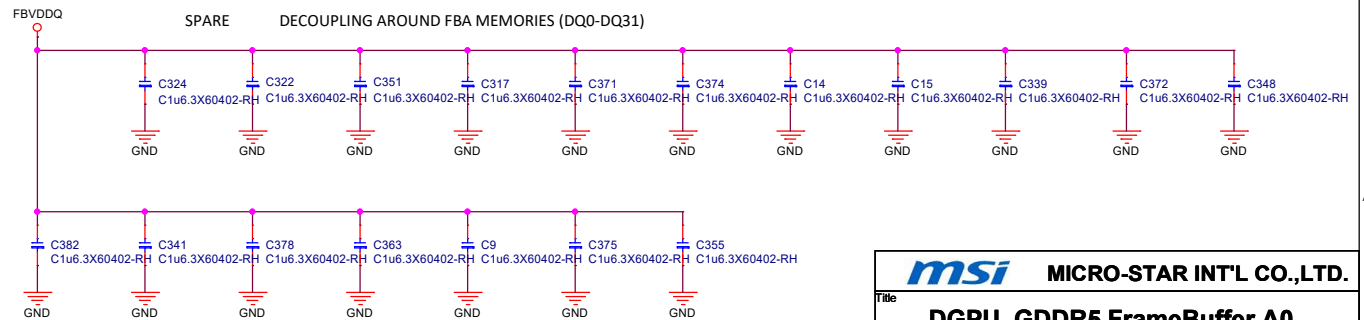
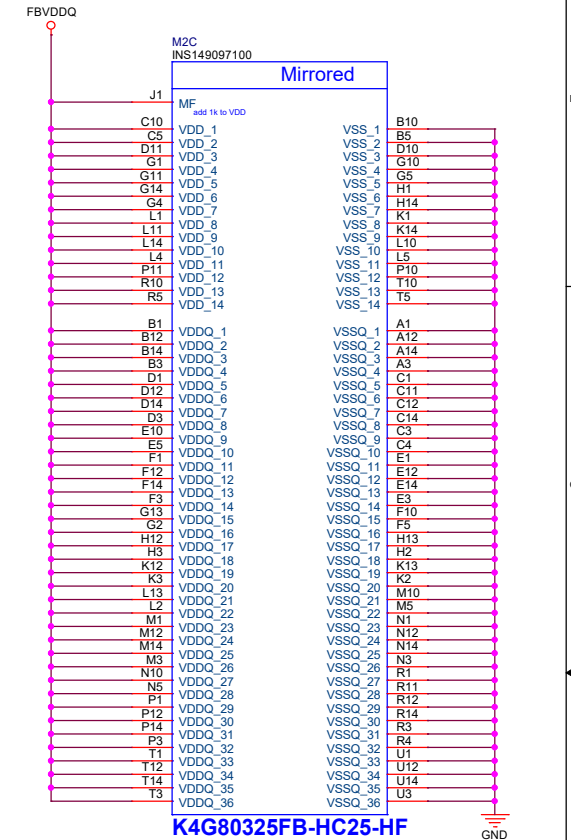
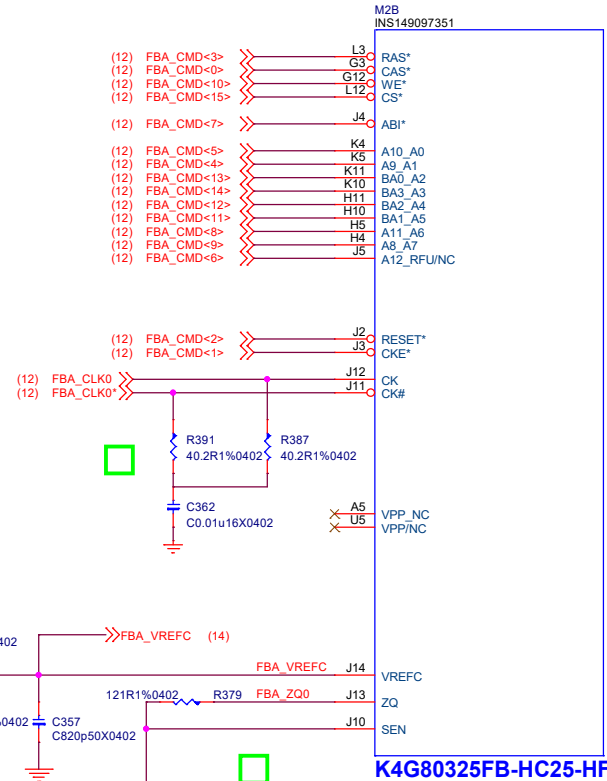
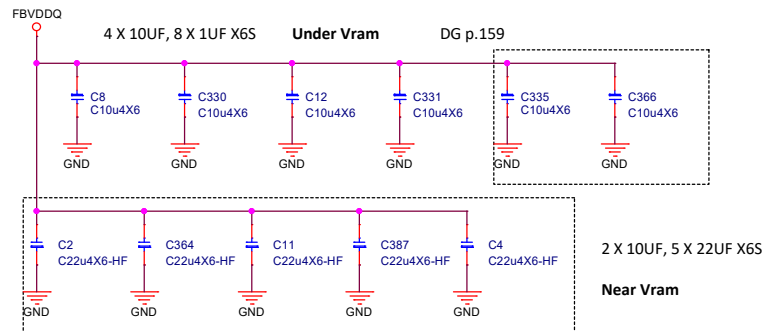
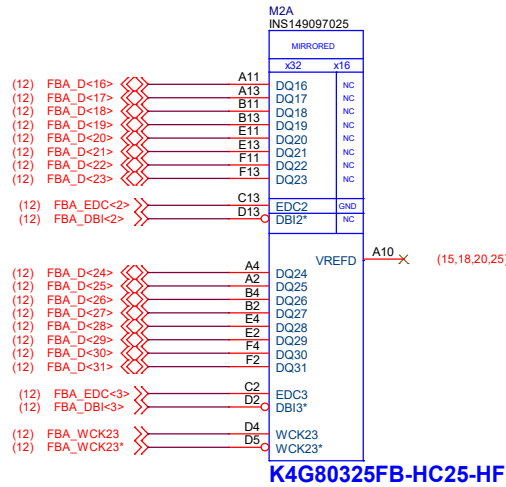
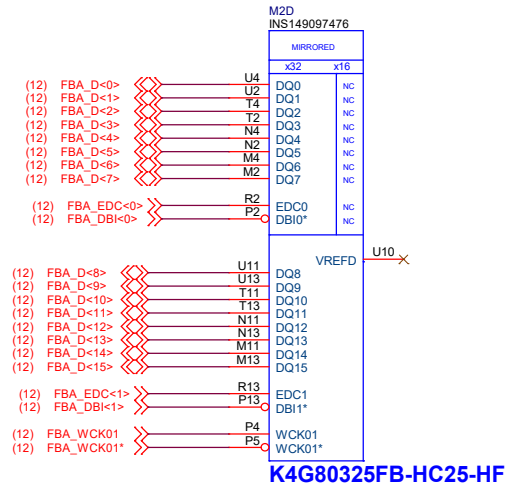


GPU Frame Buffer Partition A/B

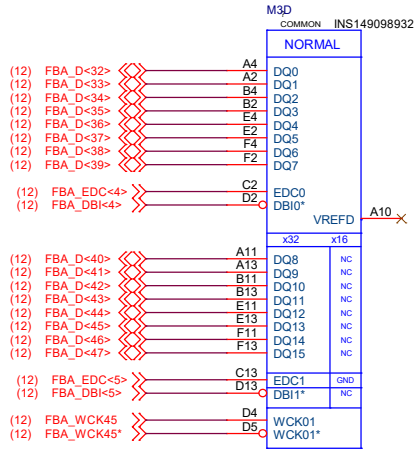


Hynix PN : M12-5GC2H05-H23 2G(64Mx32bit)
Samsung PN : M12-2032585-S02 2G(64Mx32bit)

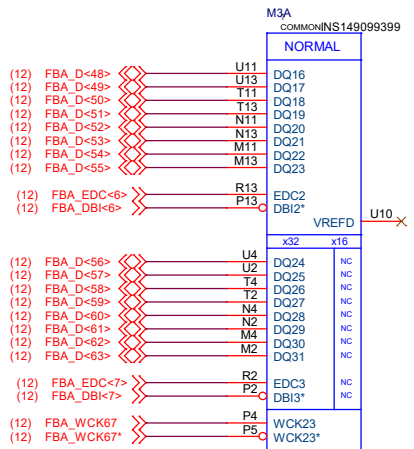
DGPU_GDDR5 FrameBuffer A0



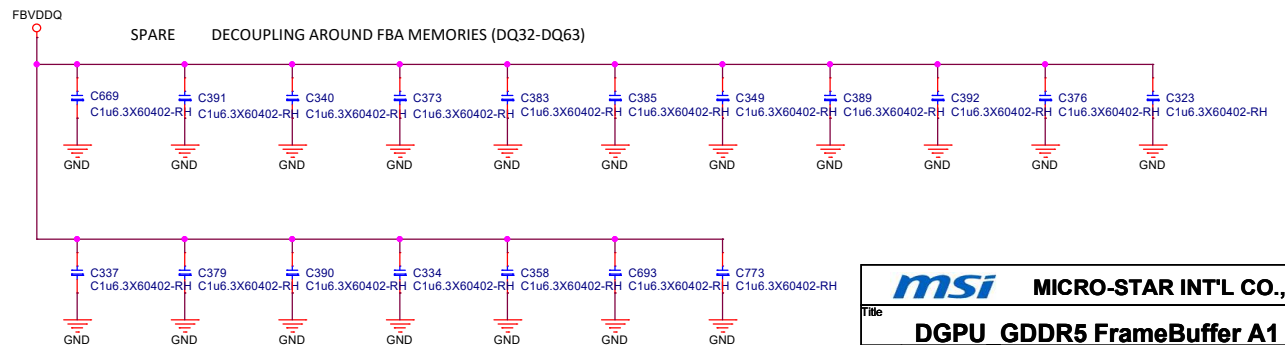
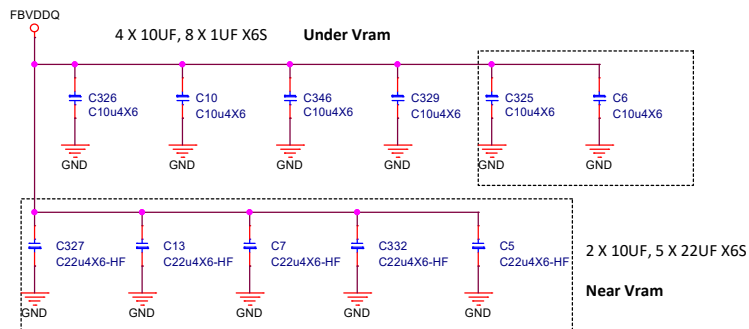
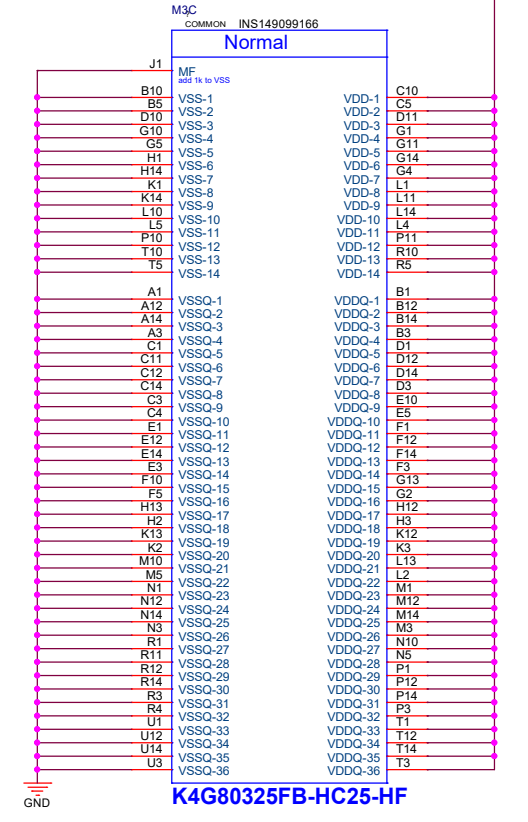
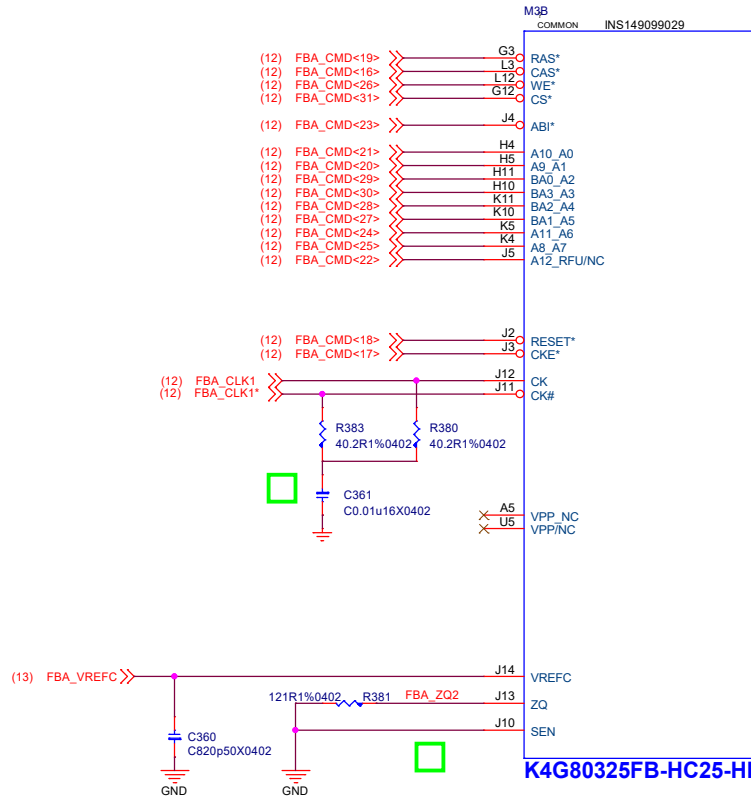
DGPU_GDDR5 FrameBuffer A1



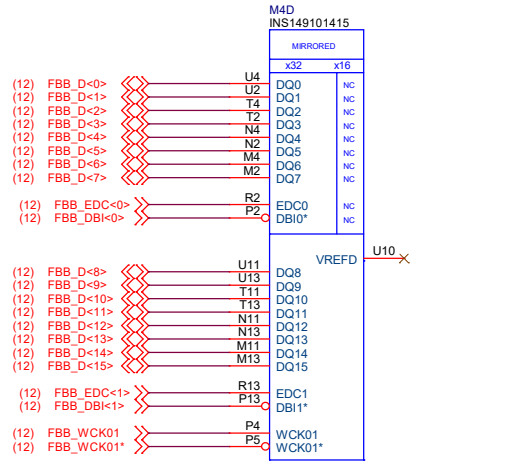
K4G80325FB-HC25-HF



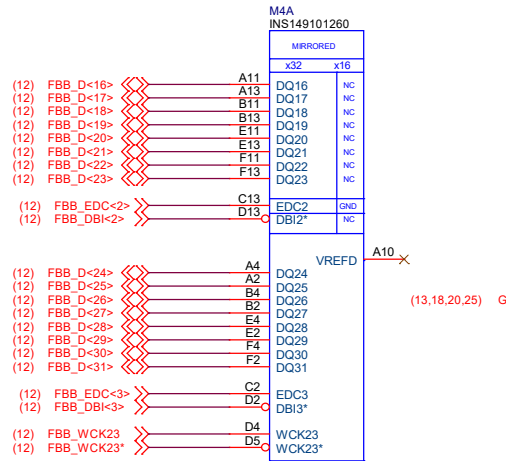
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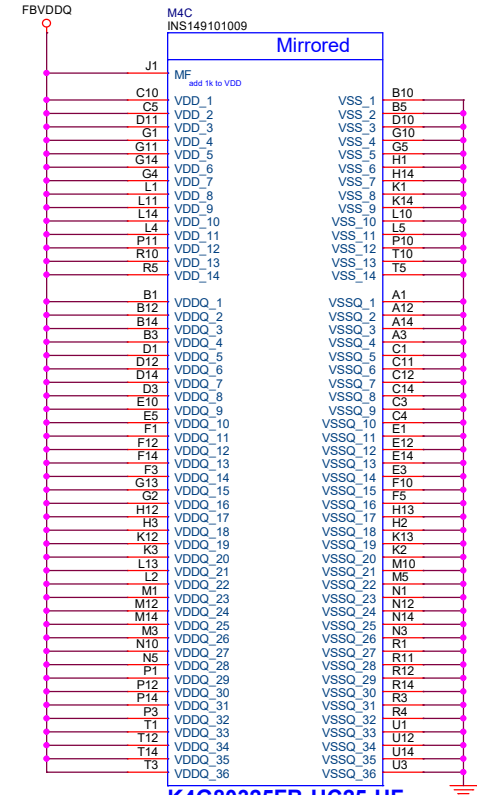
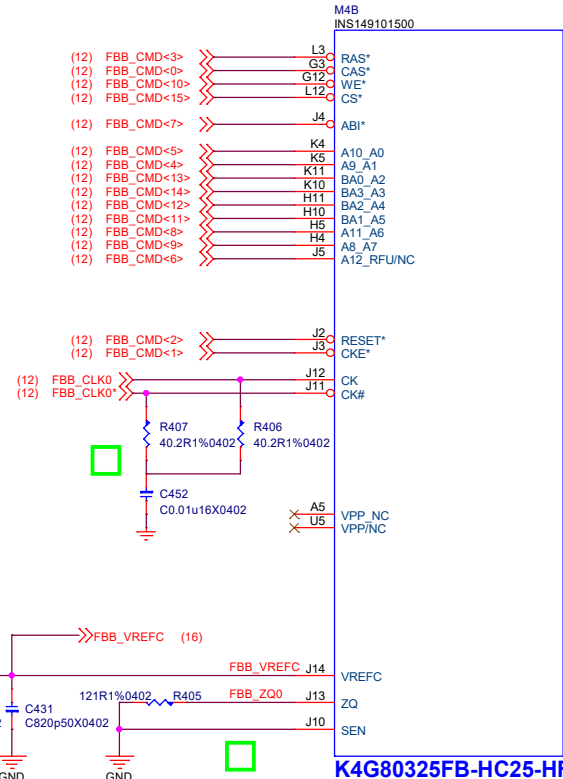
DGPU_GDDR5 FrameBuffer B0



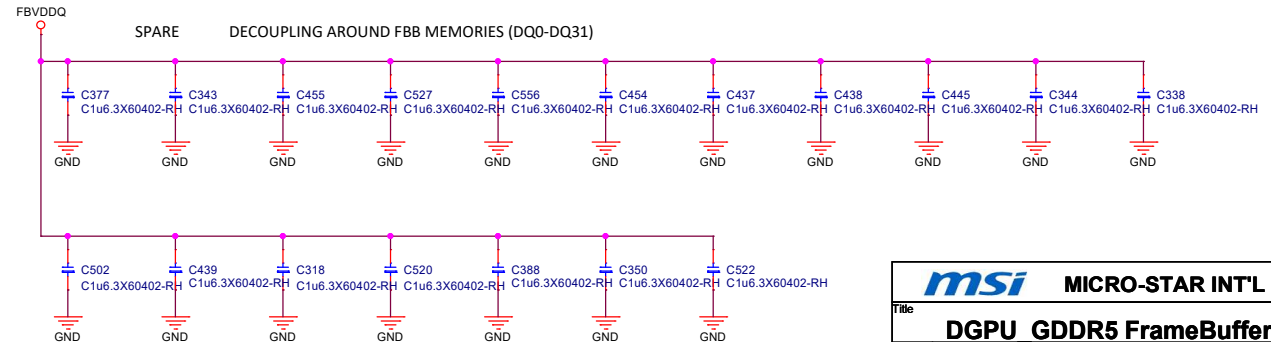
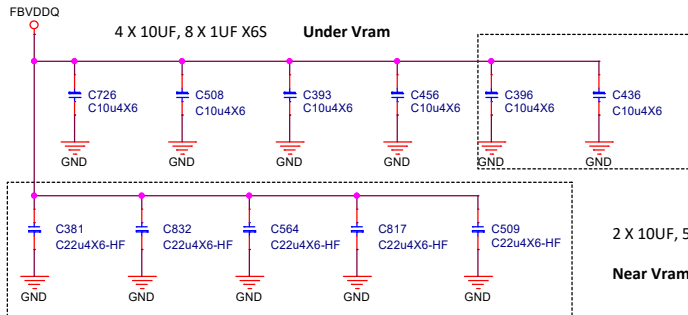
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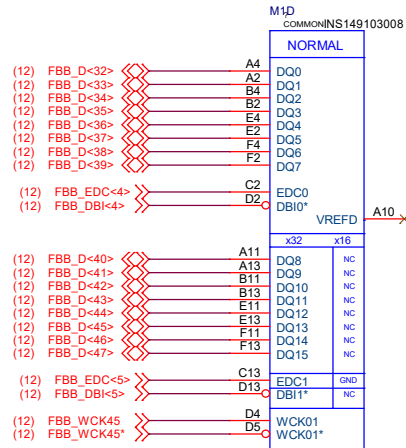
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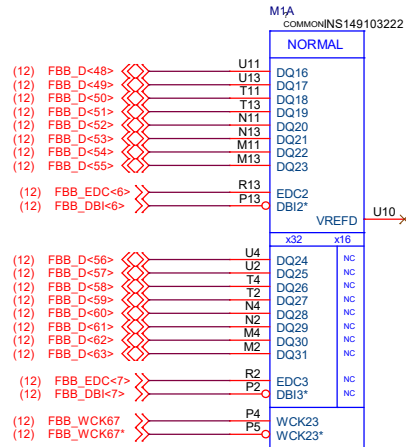
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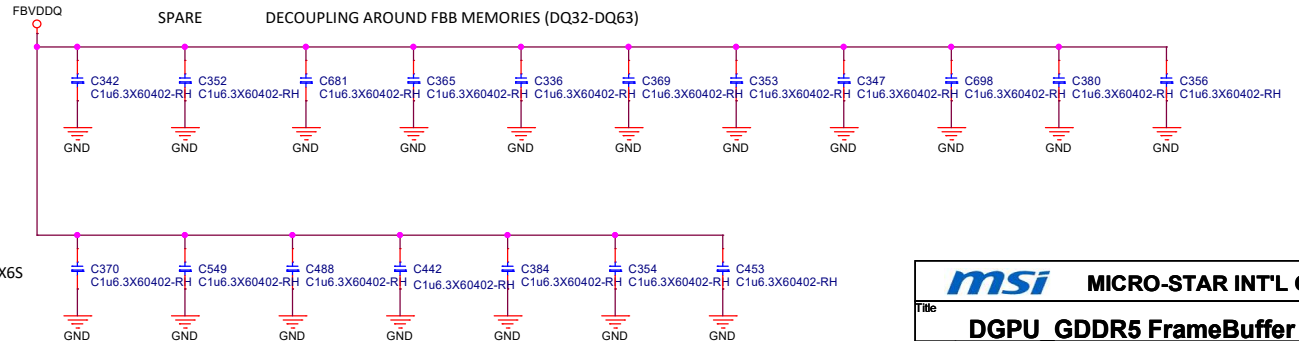
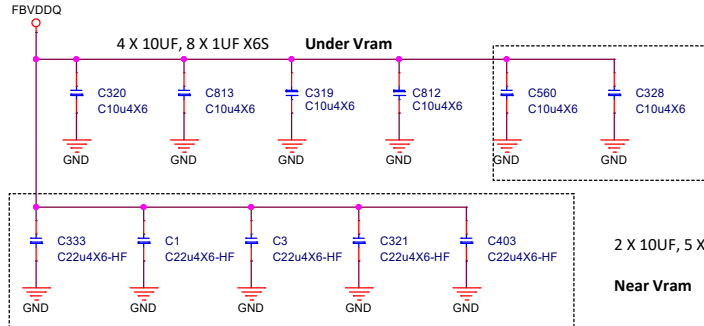
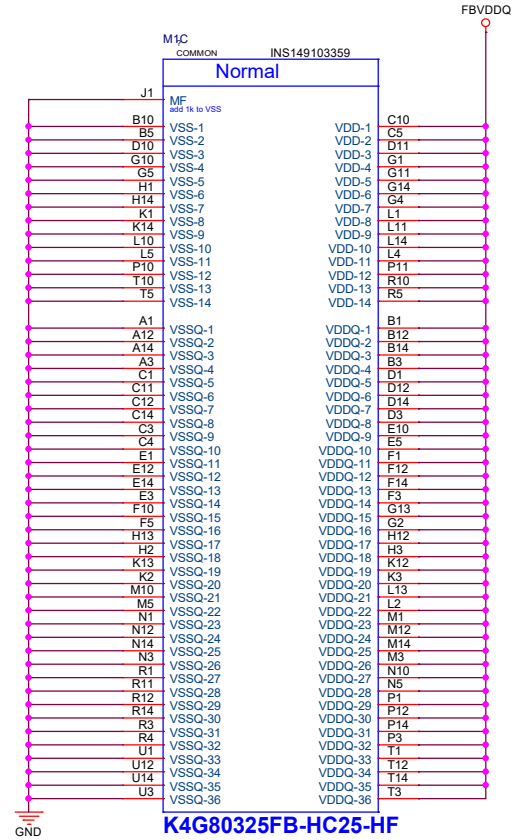
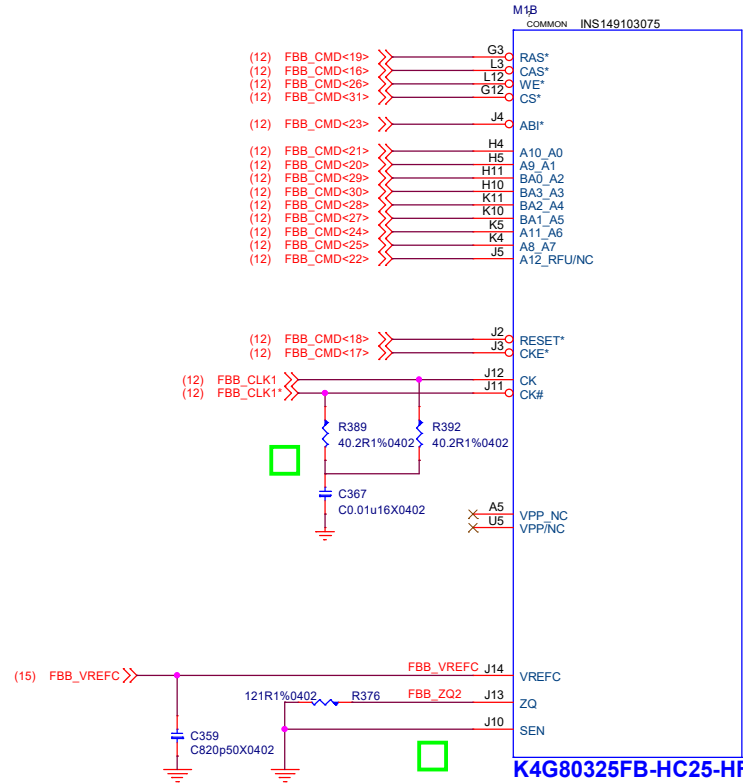
DGPU_GDDR5 FrameBuffer B1



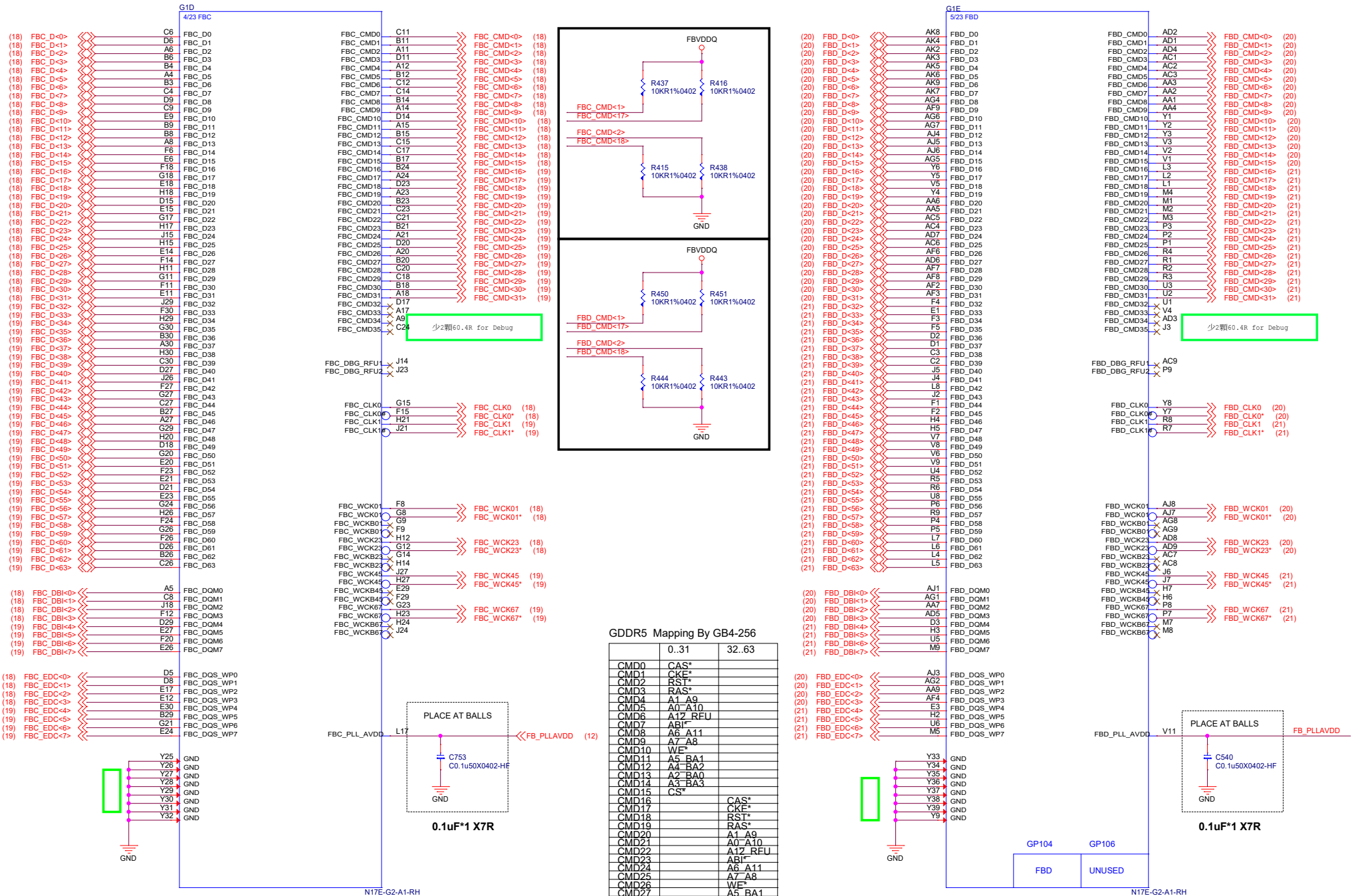
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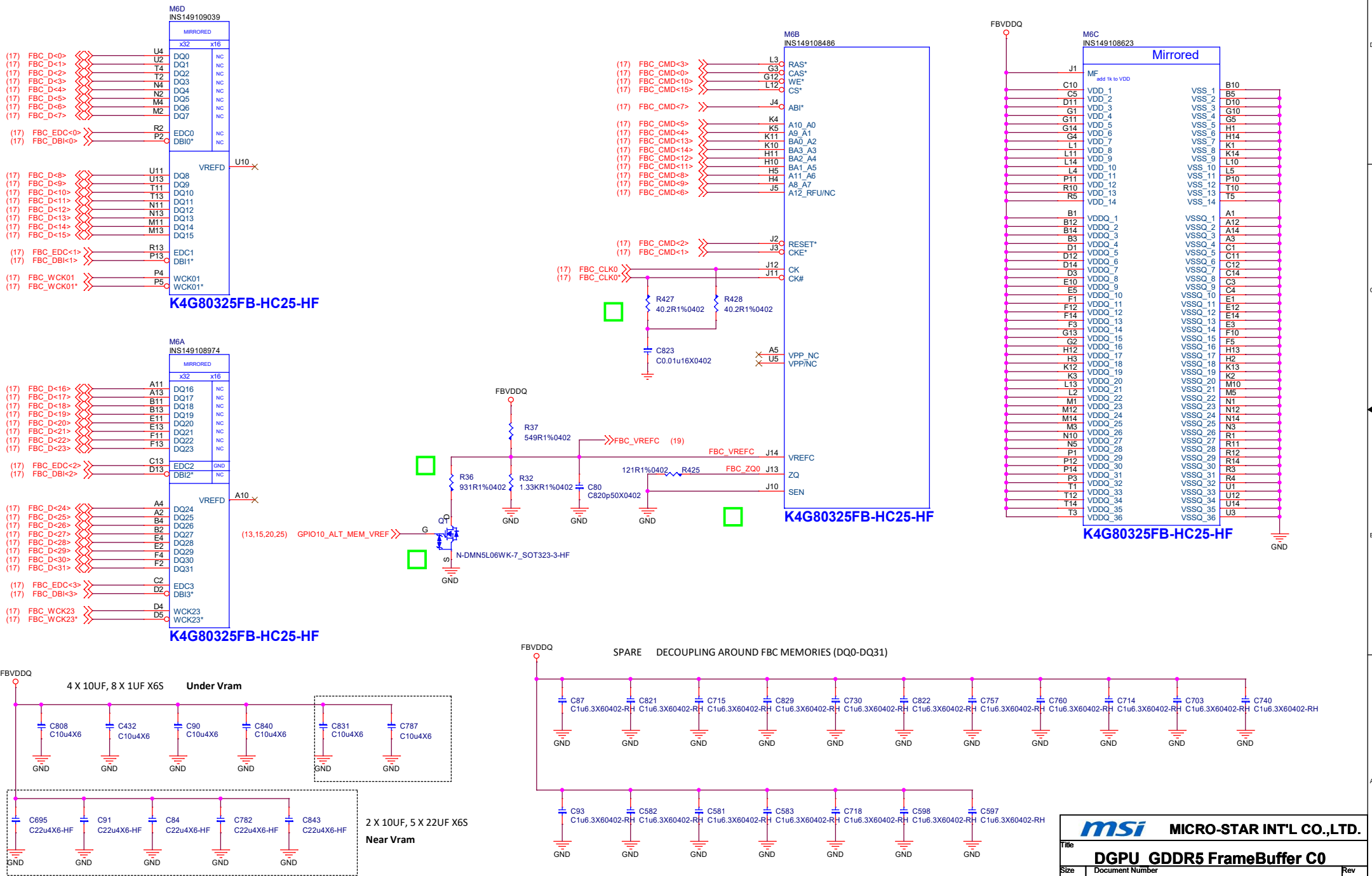
K4G80325FB-HC25-HF



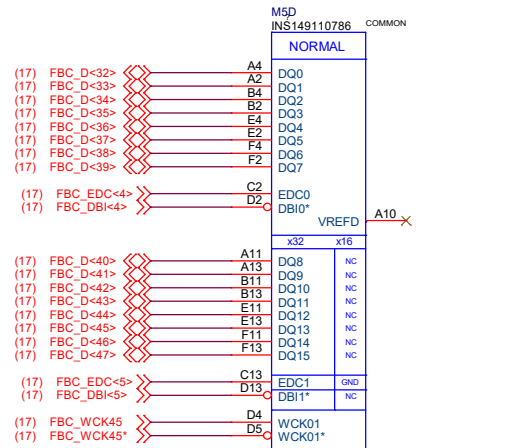
GPU Frame Buffer Partition C/D



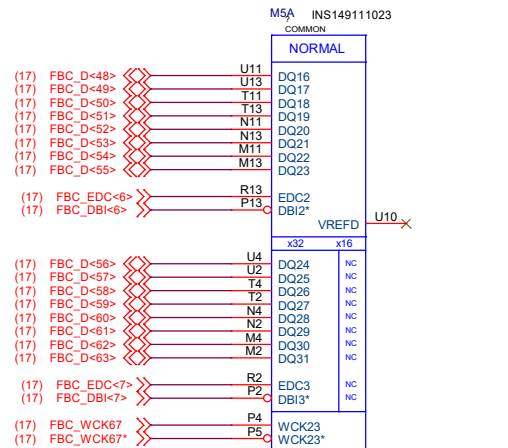
DGPU_GDDR5 FrameBuffer C0



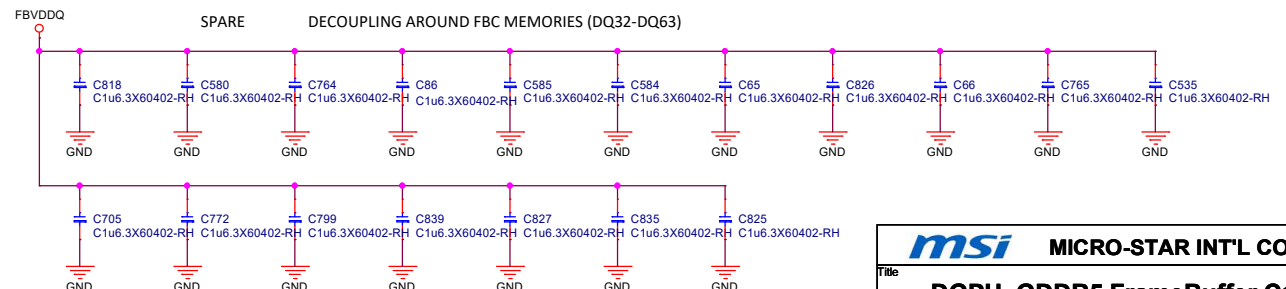
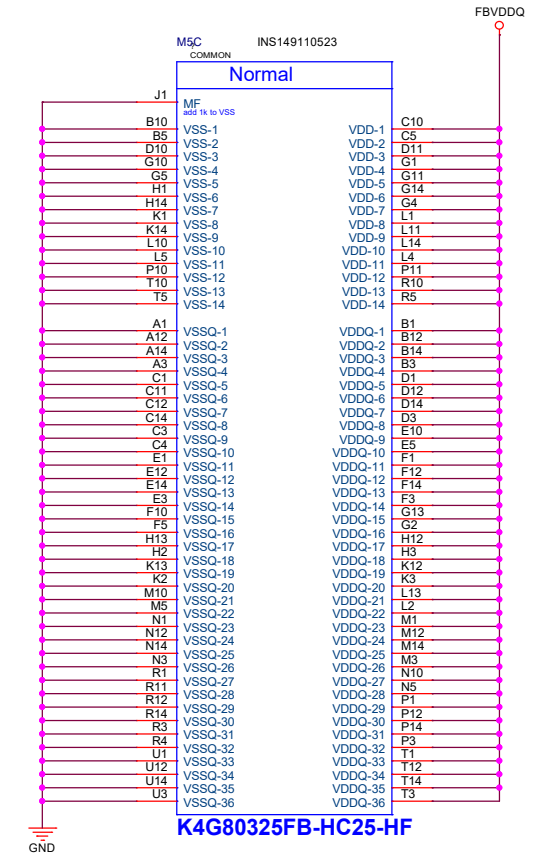
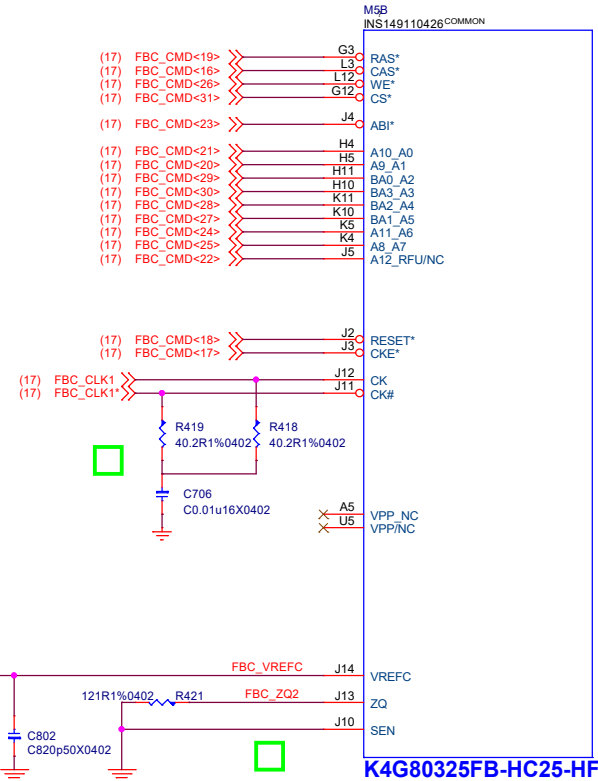
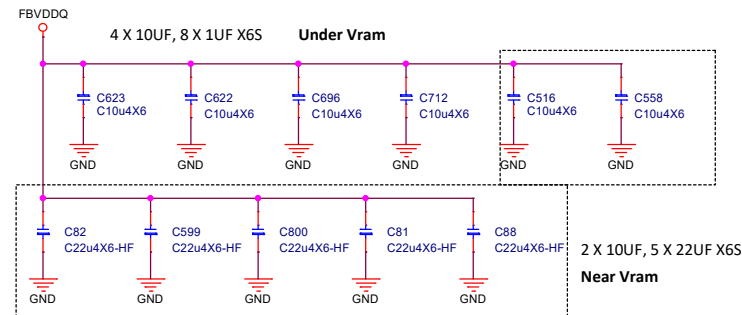
DGPU_GDDR5 FrameBuffer C1



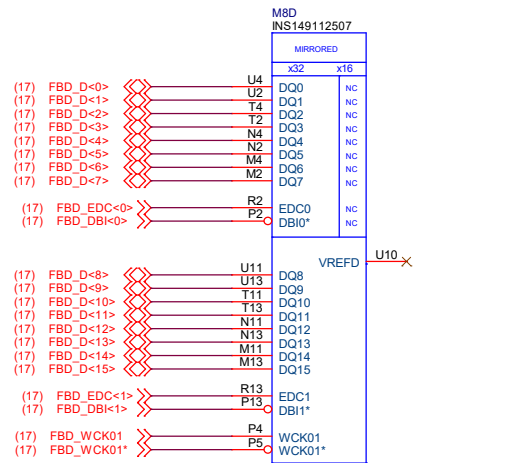
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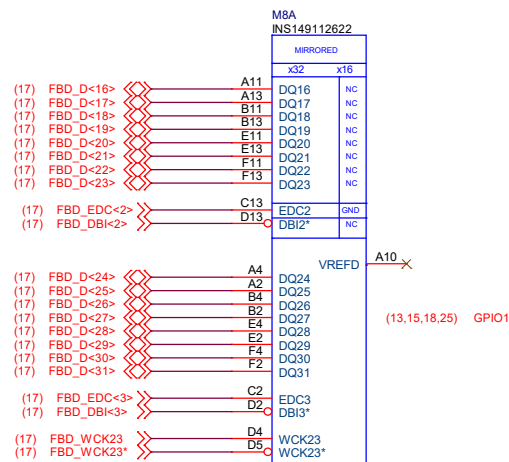
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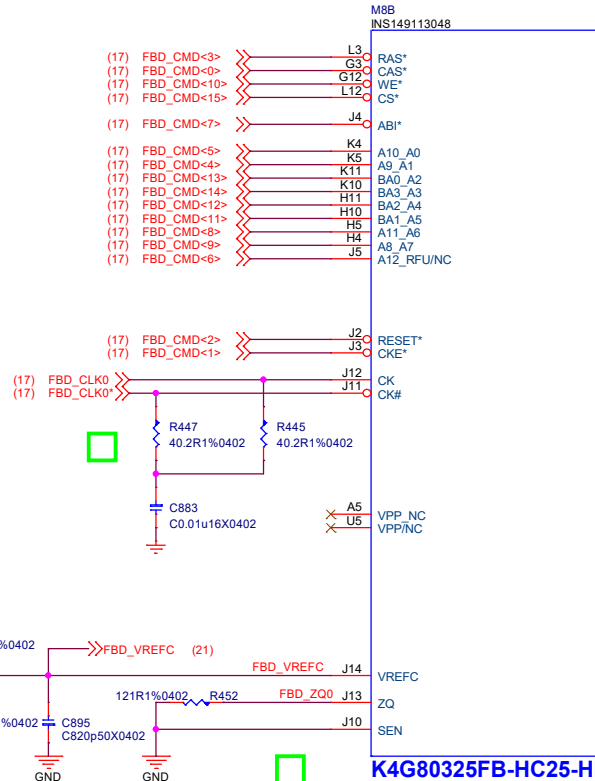
DGPU_GDDR5 FrameBuffer D0



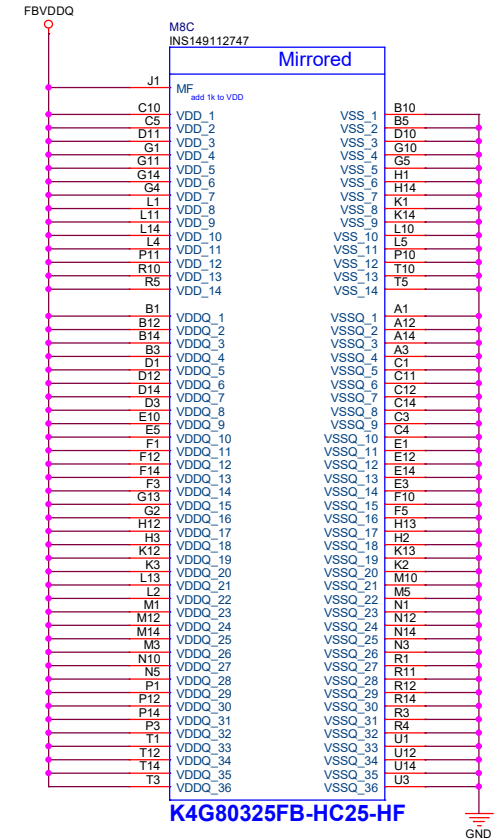
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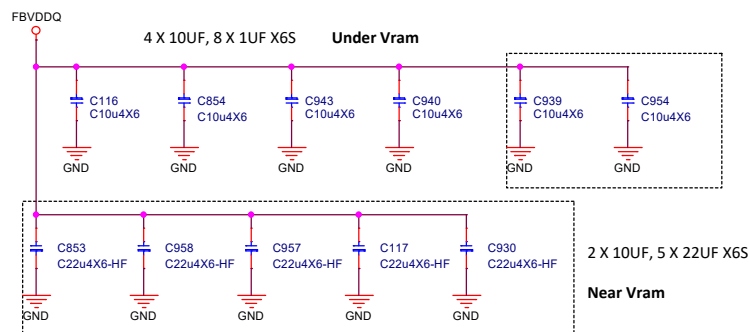
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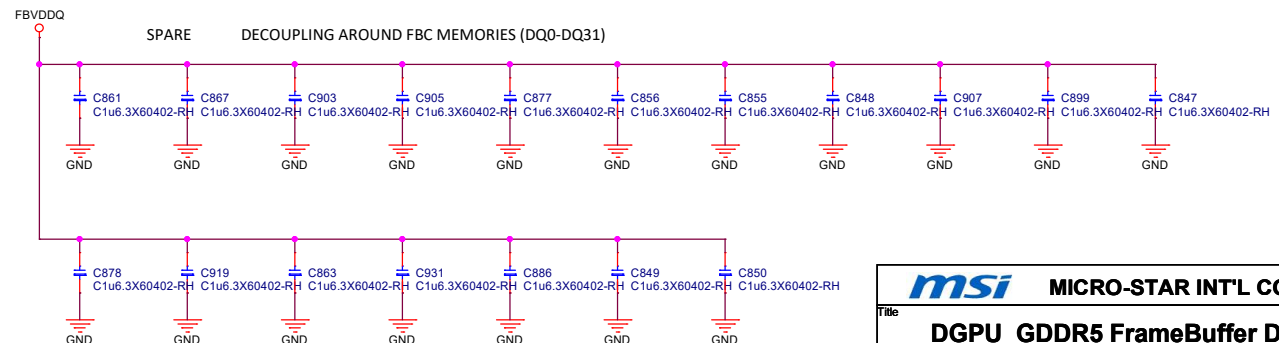
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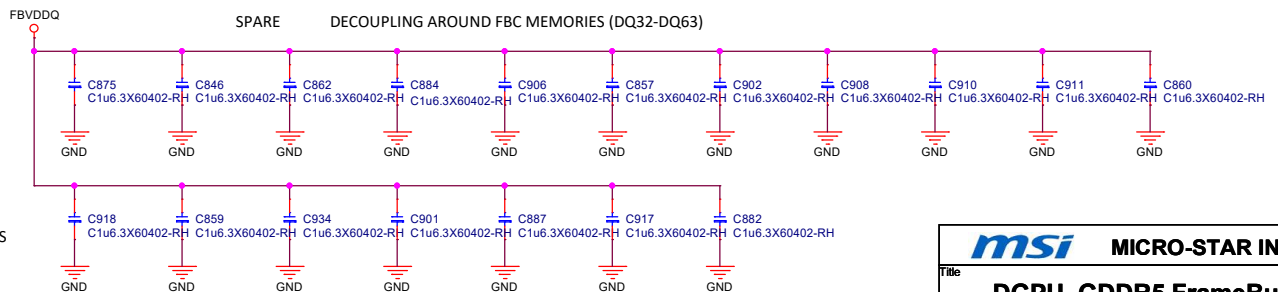
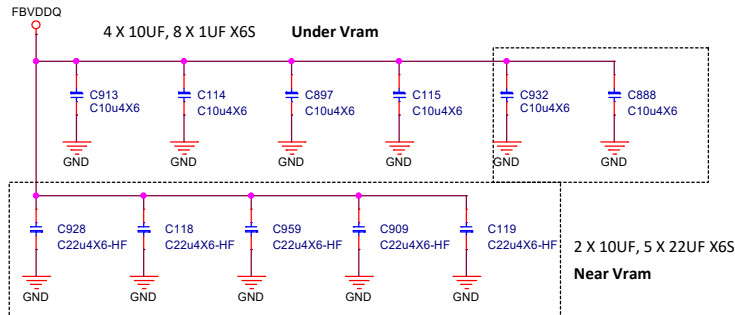
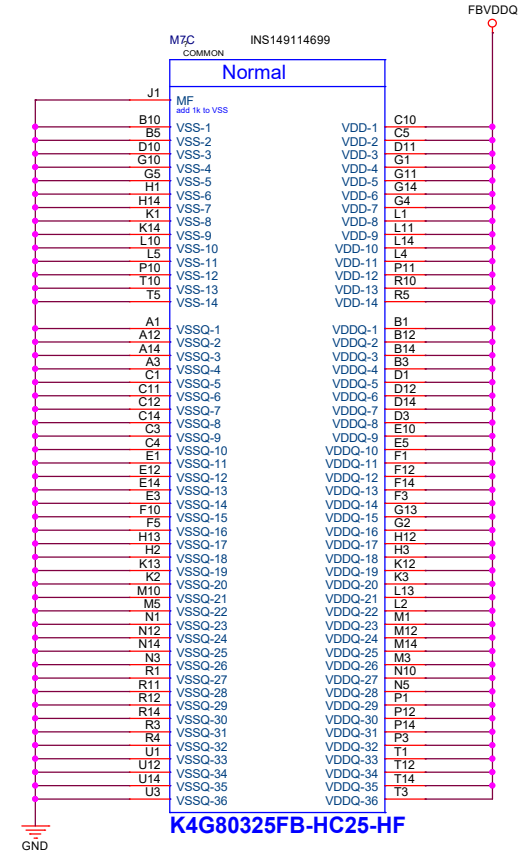
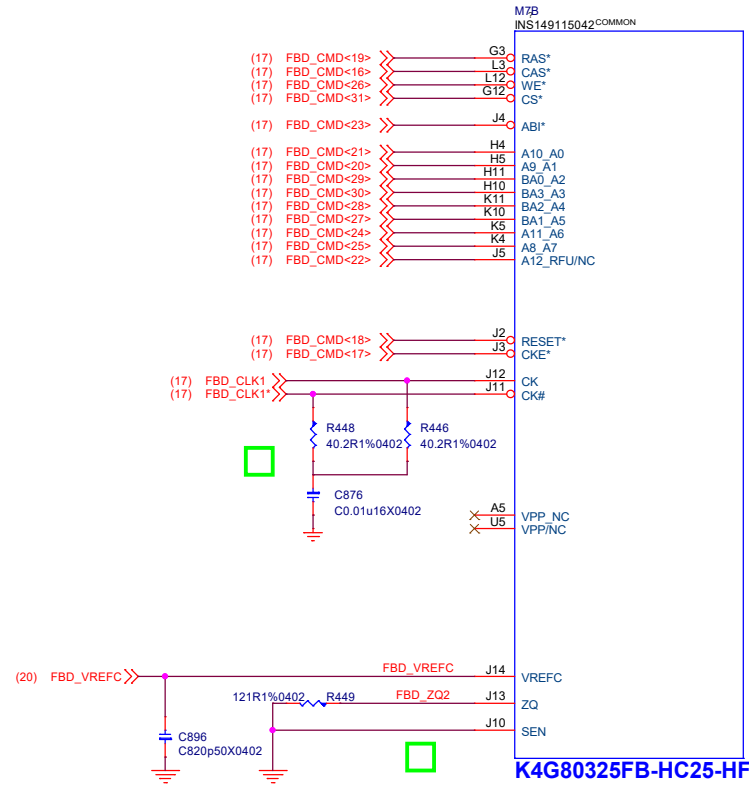
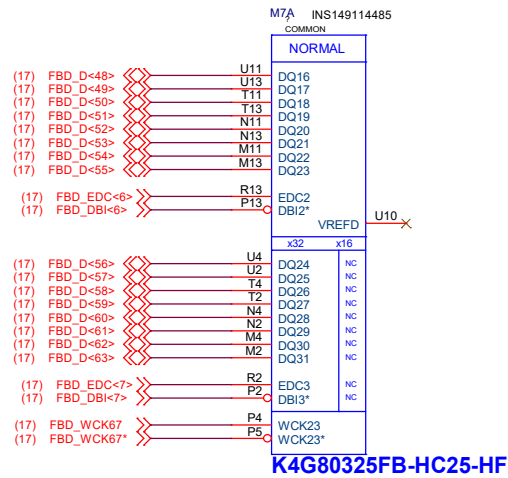
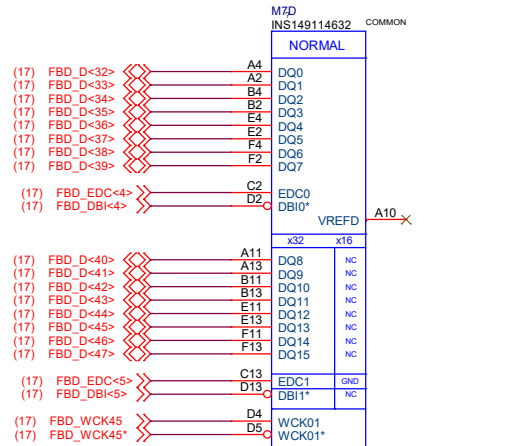
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Near Vram

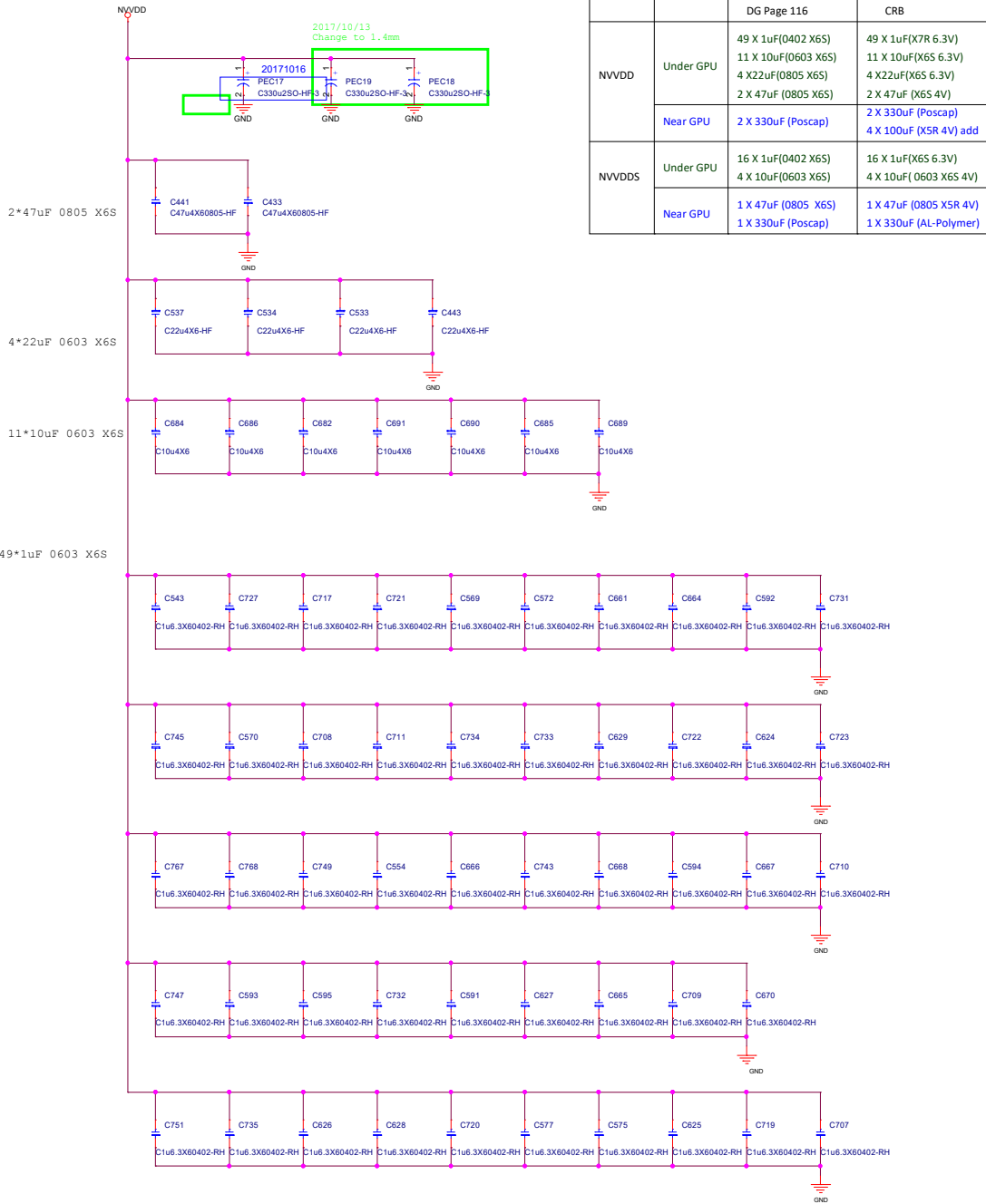


DGPU_GDDR5 FrameBuffer D1

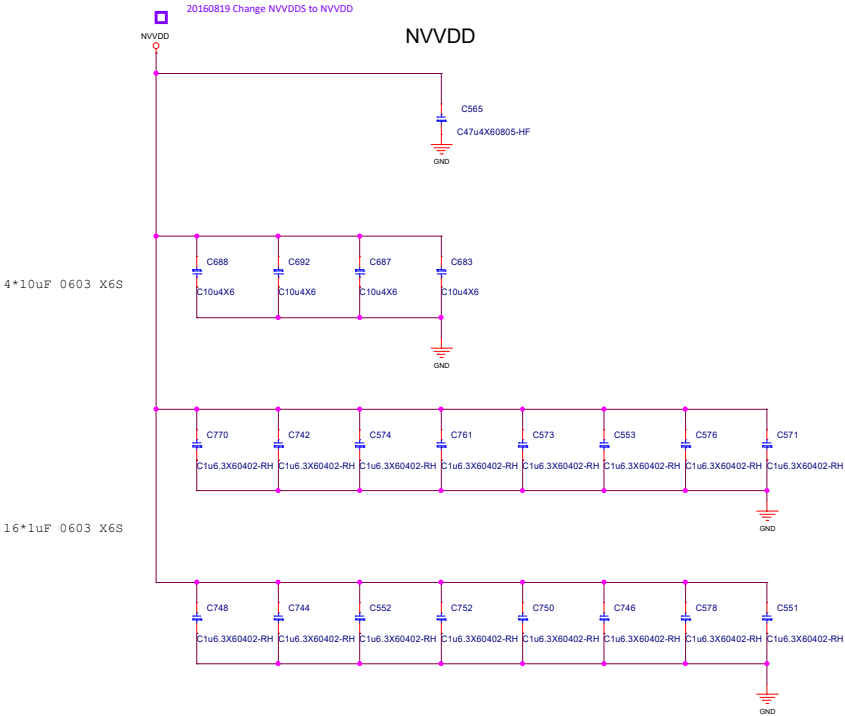


GPU DECOUPLING A

NVDD

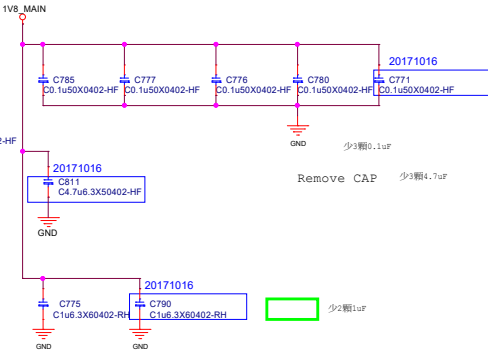


NVDD



place 1* 0.1uF cap near BA10

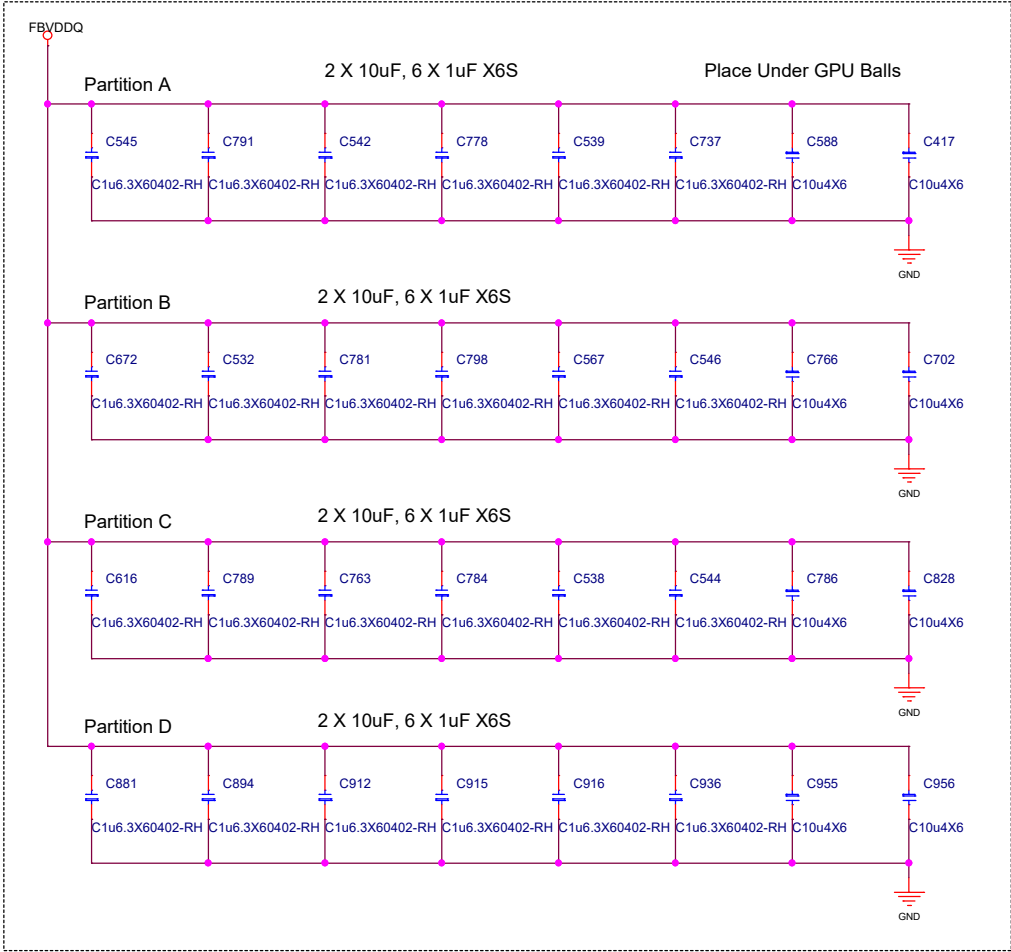
place 1* 0.1uF cap for BB14 and BC14 to share



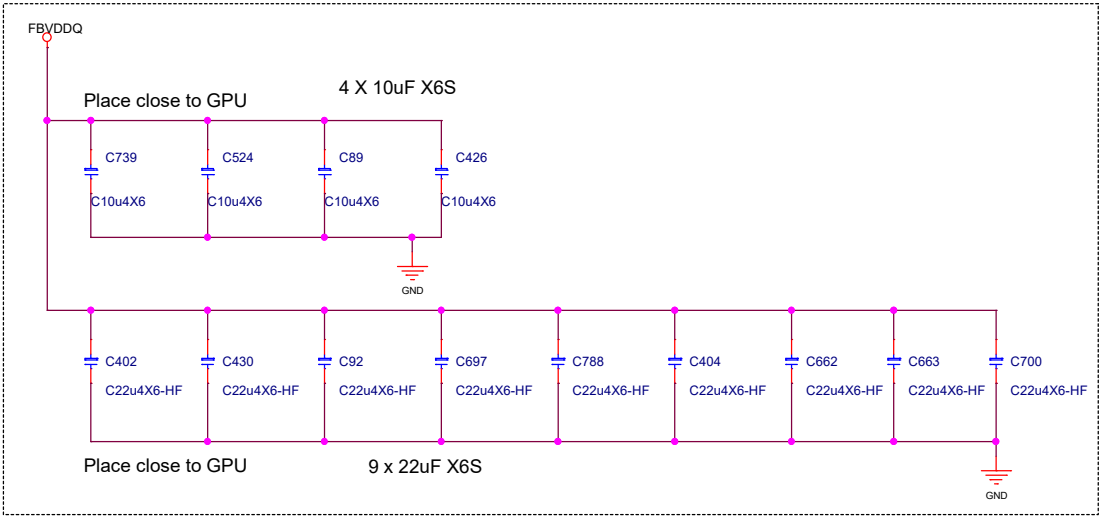
		DG Page 117	CRB
1V8_MAIN	Under GPU	7 X 0.1uF(0402)	7 X 0.1uF(0402 X7R)
	Near GPU	3 X 1uF (0402) 3 X 4.7uF (0603)	3 X 1uF (0603 X7R) 3 X 4.7uF (0603 X6S)
1V8_AON	Under GPU	2 X 0.1uF(0402)	2 X 0.1uF(0402 X7R)
	Near GPU	1 X 1uF (0402) 1 X 4.7uF (0603)	1 X 1uF (0603 X7R) 1 X 4.7uF (0603 X6S)

FBVDDQ

GPU DECOUPLING B

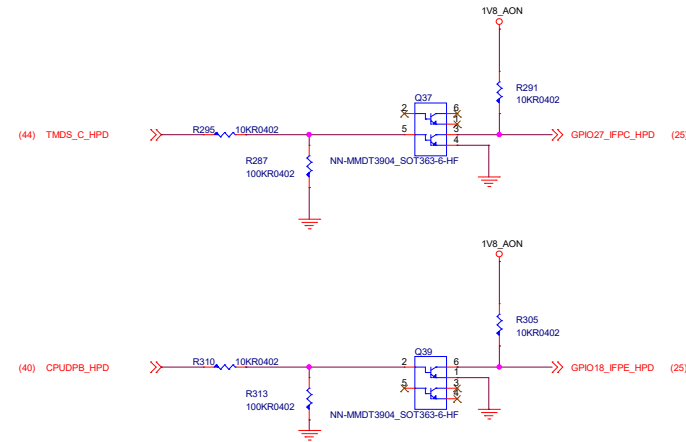
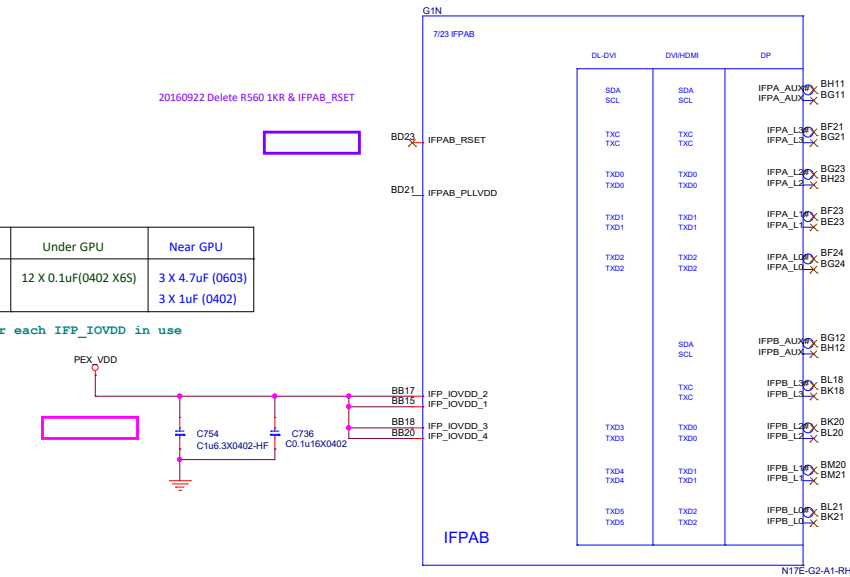


		DG Page 116	CRB
FBVDDQ (GPU side)	Under	24 X 1uF(0402 X6S) 5 X 10uF(0603 X6S)	24 X 1UF(0402 X6S 6.3V) 5 X 10uF(X6S 4V)
	Near	7 X 10uF(0603 X6S) 9 X 22uF(0603 X6S)	7 X 10uF(0603 X6S 4V) 9 X 22UF(0603 X6S 4V)

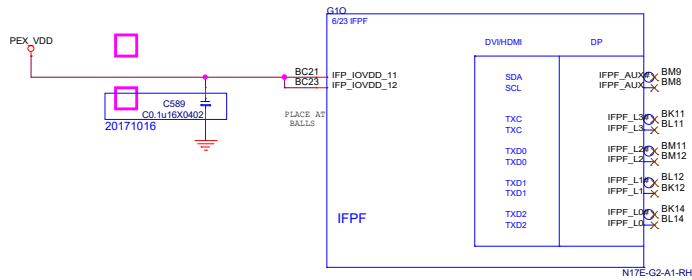
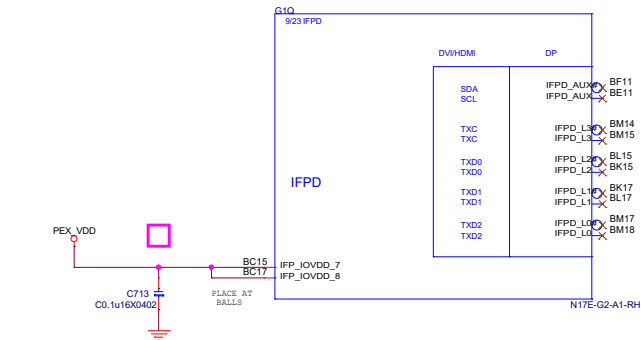
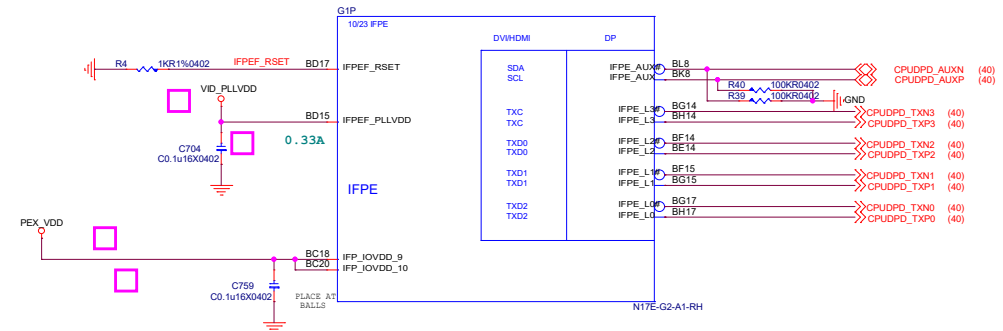
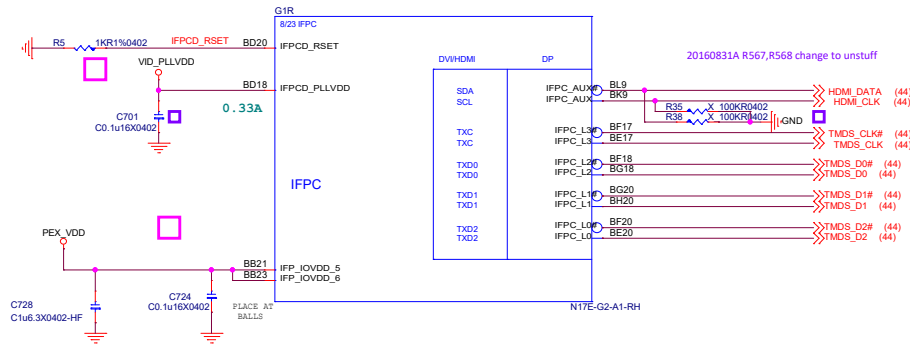


DG Page 117	Under GPU	Near GPU
IFP_IOVDD	12 X 0.1uF(0402 X6S)	3 X 4.7uF (0603) 3 X 1uF (0402)

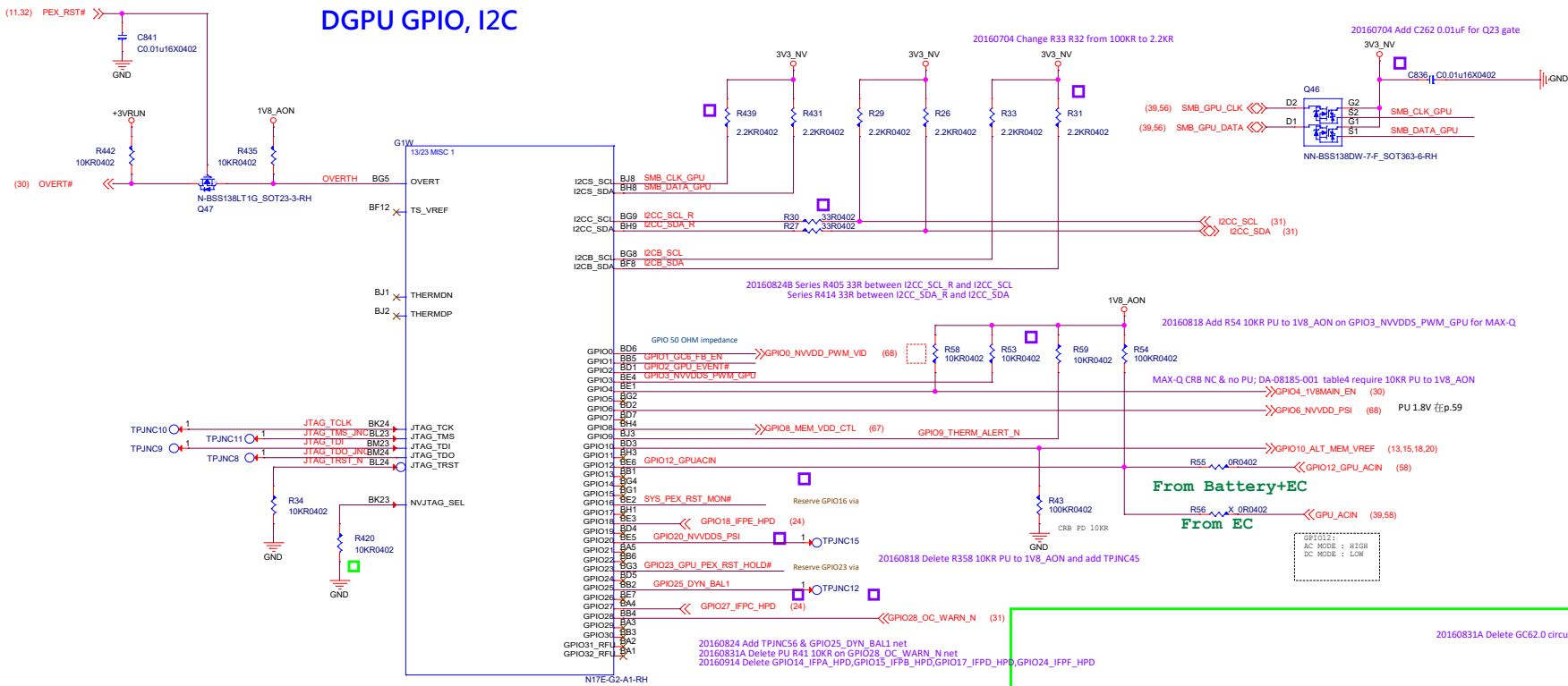
0.305A for each IFP_IOVDD in use



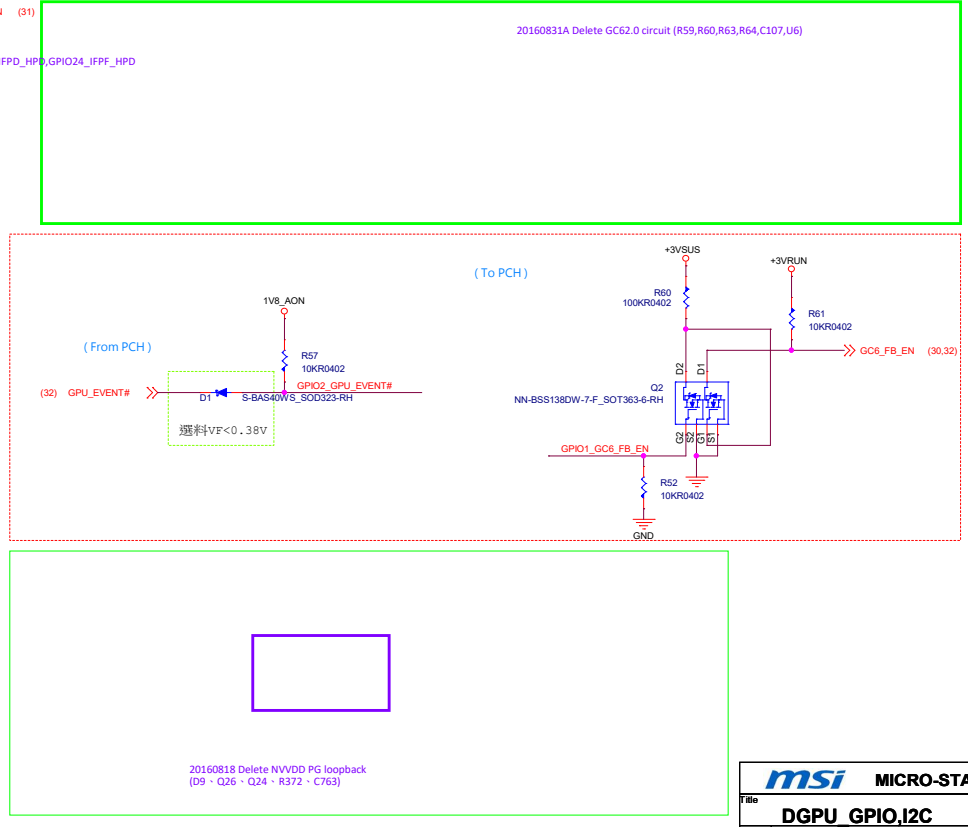
20160914 Delete R562, R564, R565, R583 & GPIO14_IFPA_HPD, GPIO15_IFPB_HPD, GPIO17_IFPD_HPD, GPIO24_IFPE_HPD



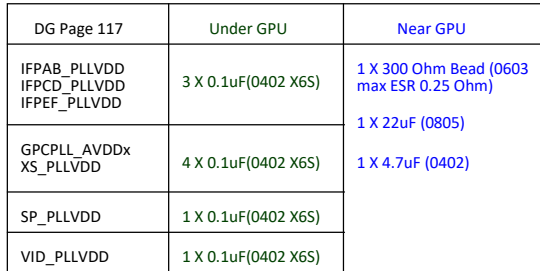
DGPU GPIO, I2C



Pin Number	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to 1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source, 10K pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDDS_PWM	O	PWM output to control the NVVDDS power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8_AON
GPIO5	FRM_LCK#	I	Active low Fram Lock	OD, 10K pull-up to 1V8_AON
GPIO6	NVVDD_PSI#/NVVDDS_PSI#	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight enable control signal to turn on a logo LED	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT#	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD; Quadro: Power_Brake#	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	
GPIO14	HPD_IFPA#	I	Hot Plug Detect for IFPA	Inverted input
GPIO15	HPD_IFPB#	I	Hot Plug Detect for IFPB	Inverted input
GPIO16	GC6M: SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 1V8_AON
GPIO17	HPD_IFPD#	I	Hot Plug Detect for IFPD	Inverted input
GPIO18	HPD_IFPE#	I	Hot Plug Detect for IFPE	Inverted input
GPIO19	3Dvision/STEREO	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE	I/O		
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI Swap Ready Out	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset control	OD, 10K pull-up to gated 3V3
GPIO24	HPD_IFPF#	I	Hot Plug Detect for IFPF	Inverted input
GPIO25	Unused	I/O		
GPIO26	Unused	I/O		
GPIO27	HPD_IFPC#	I	Hot Plug Detect for IFPC	Inverted input
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10K pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	Unused	I/O		

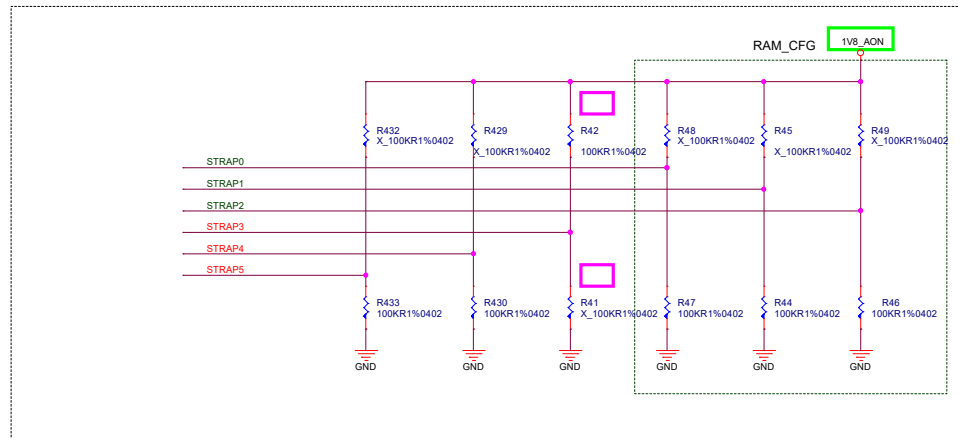
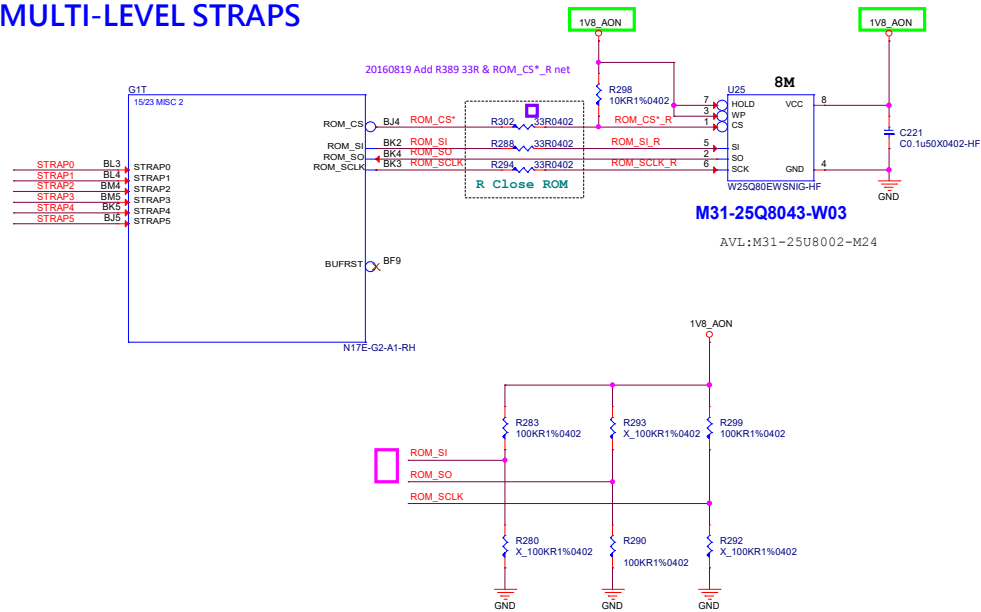


20160704 Add C1041 22uF & C1038 4.7uF & C1040 0.1uF for VID_PLLVDD
20160912A Delete C1041 & C1038



The image displays two schematic diagrams for connecting MIO and MIOB pins to a microcontroller. The left diagram shows the MIO pins (G1V) connected to various signals, including MIOACAL_PD_VDDQ, MIOACAL_PU_GND, MIOA_VREF, and MIOA_CTL3. The right diagram shows the MIOB pins (G1U) connected to signals like MIOBCAL_PD_VDDQ, MIOBCAL_PU_GND, MIOB_VREF, and MIOB_CTL3. Both diagrams include a 1KR1%0402 resistor and a 100pF capacitor for timing.

ROM, MULTI-LEVEL STRAPS



V_TOP1		5010	256M*32
DEFAULT SETTING	<input checked="" type="checkbox"/>	M12-8032535-S02	
SAMSUNG	<input type="checkbox"/>	X_K4G80325FB-HC25-HF	
V_TOP2		5010	256M*32
MICRON	<input checked="" type="checkbox"/>	M12-2563215-M30	
	<input type="checkbox"/>	X_MT51J256M32HF-80-A-HF	
20160817 Delete V_TOP3 M12-5GQ4H45-H23 and V_TOP4 M12-41325D5-S02			

STRAP2	STRAP1	STRAP0	RAMCFG[2:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

256M*32
SAMSUNG 0X0
MICRON 0X1
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	V
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

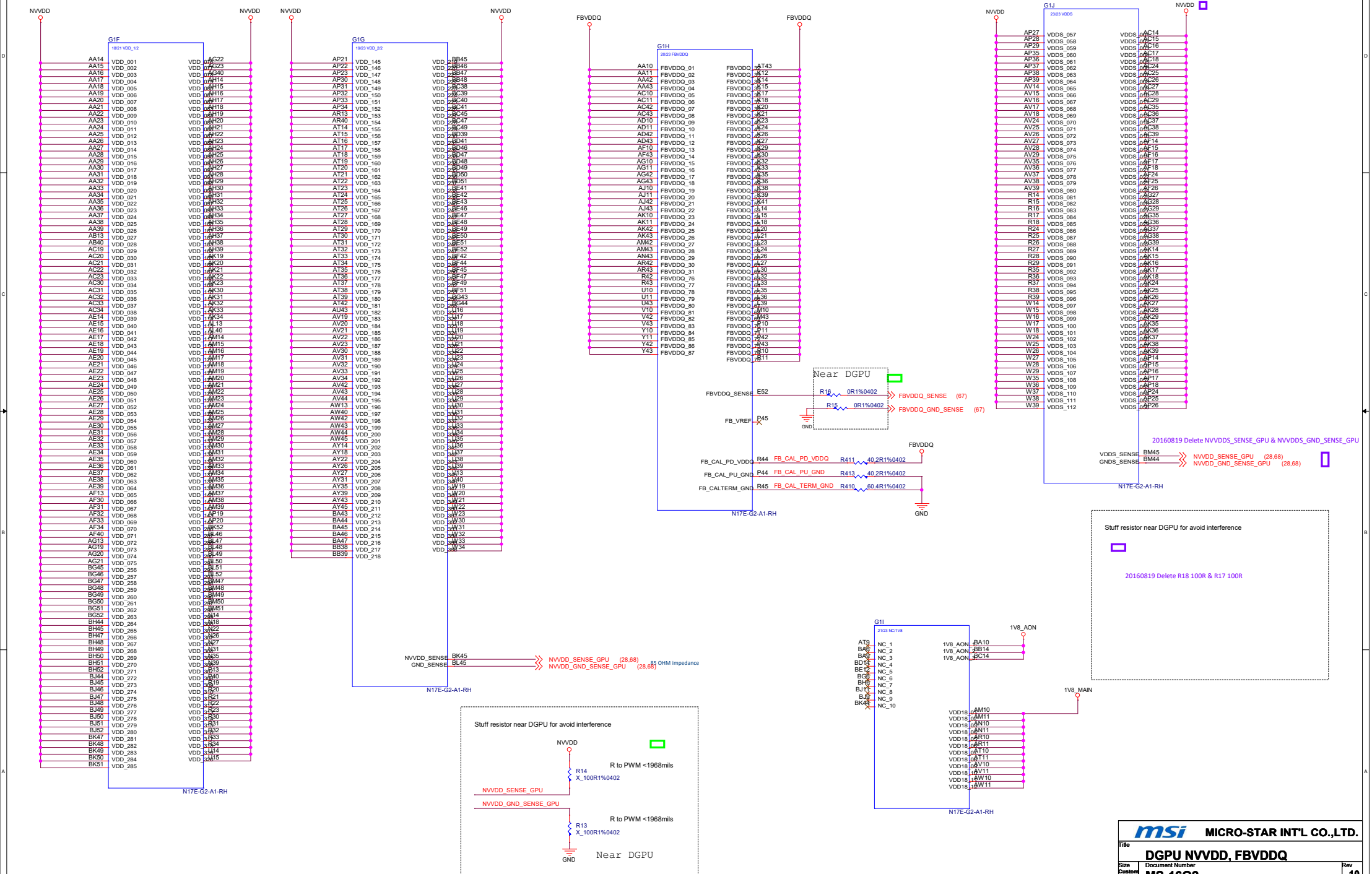
SOR_EXPOSED :GPU AUDIO SETTING

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

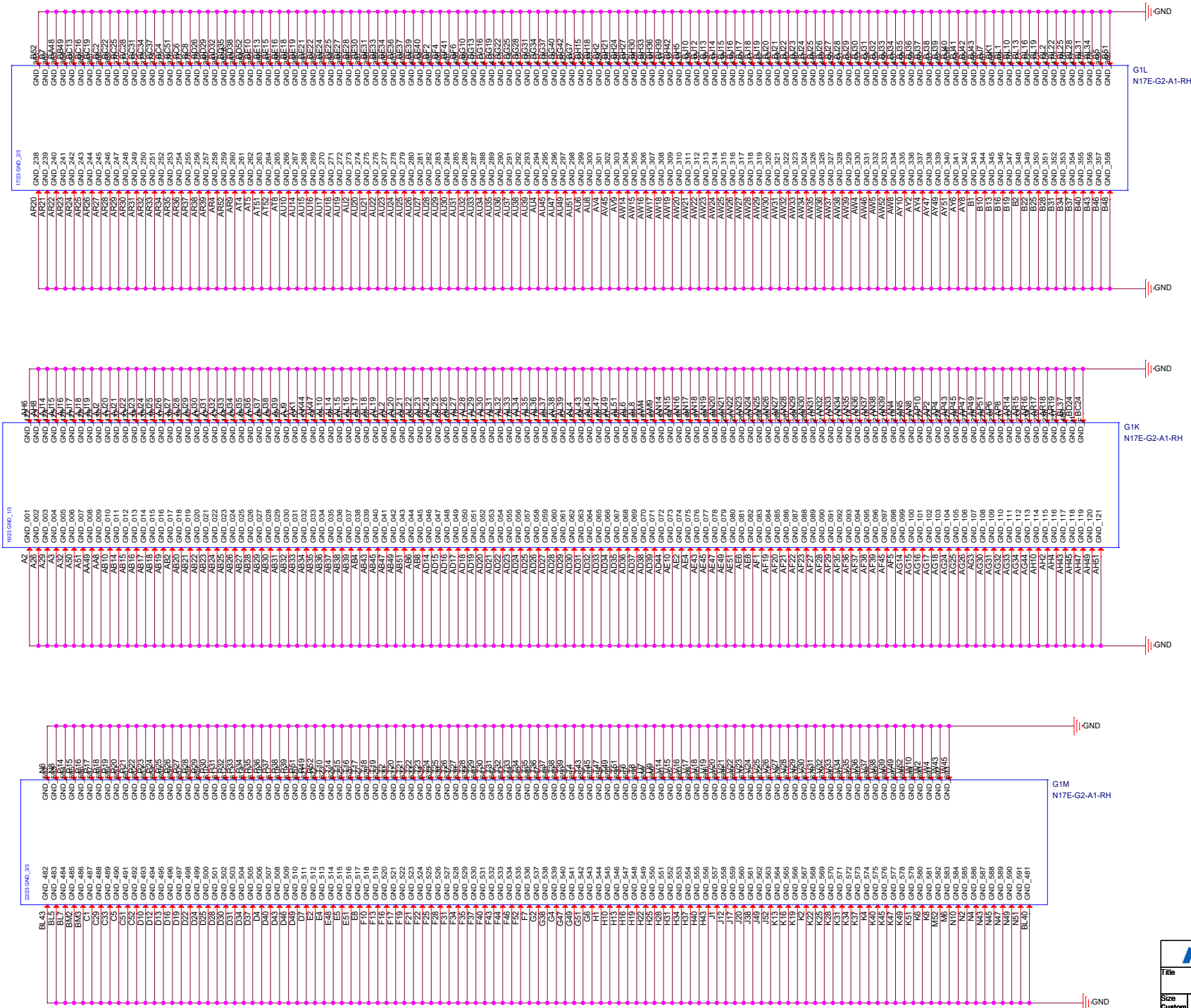
1:SMB_ALT_ADDR ENABLE (DUAL GPU)
0:SMB_ALT_ADDR DISABLE (SINGLE GPU)
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW SWING POWER
0:PCIE_CFG HIGH SWING POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

GPU NVVDD, FBVDDQ

20160819 Change VDDS connect to NVVDD



DGPU GND

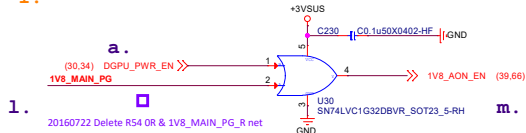


nVIDIA Power Sequence Control

Power on = 1V8_AON ->1V8_MAIN->3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power off= DGPUPWREN->(PEX_VDD->NVVDDQ->3V3_NV)->FBVDDQ->1V8_MAIN->1V8_AON

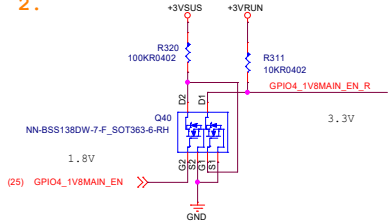
1.



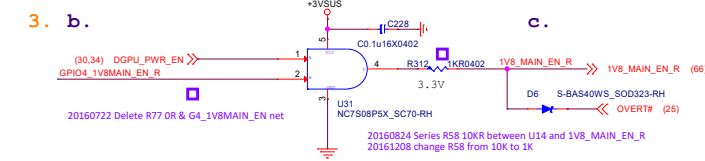
1.

20160722 Delete R54 OR & 1V8_MAIN_PG_R net

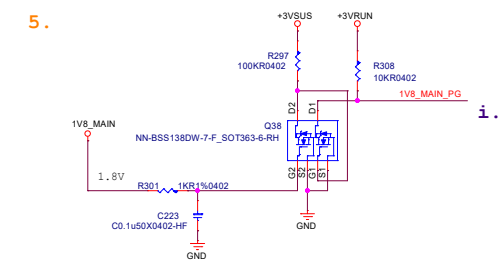
2.



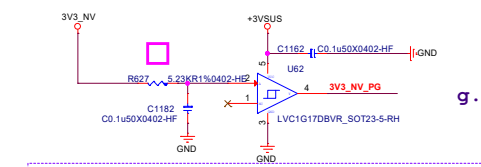
3.



5.



7.

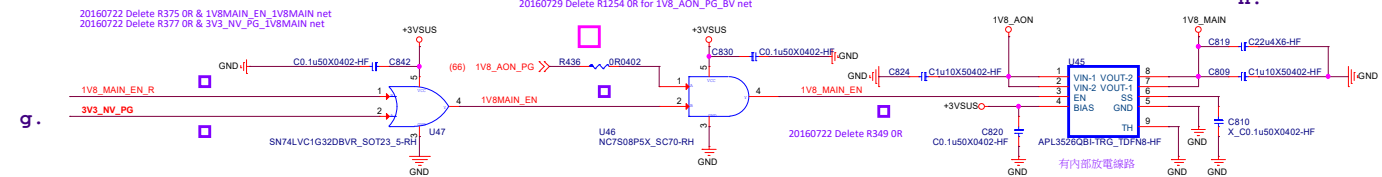


1V8_AON Power Good By Voltage and delay

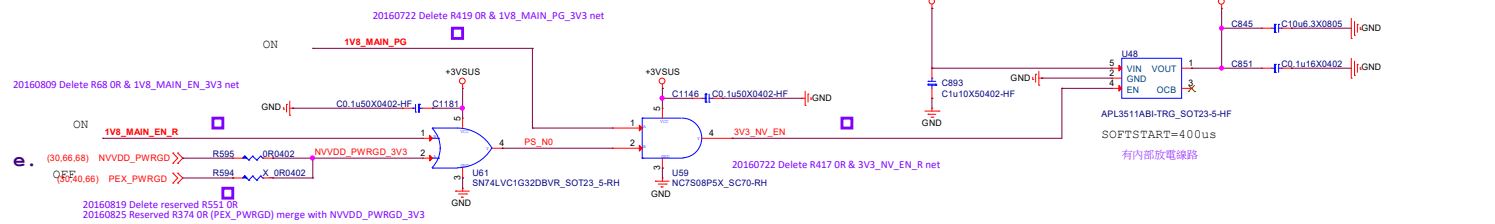
20160729 Delete U74 - C2892 - C8601 - R605 for 1V8_AON_PG_BV ent

The ramp time for any rail must be more than 40us and is recommended to be less than 2ms
From 1V8_MAIN_EN to PEX_VDD must NOT exceed 4ms

4.



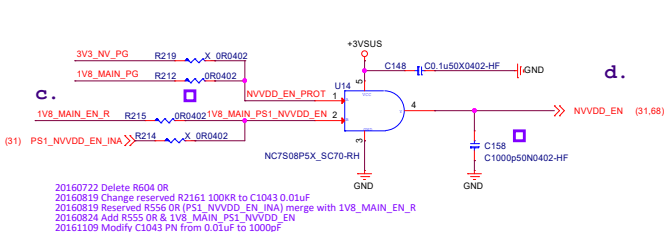
6.



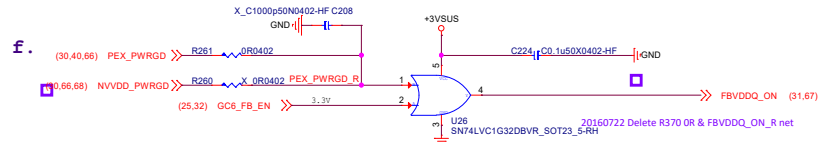
NVVDD Power Enable

The propagation delay between 1V8_MAIN_EN and the NVVDD_EN needs to be less than 300us during both power up and power down

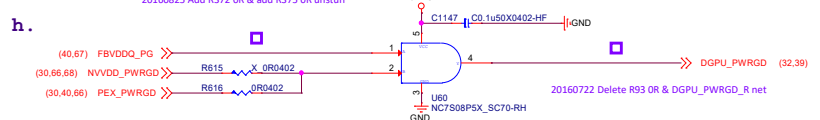
8.



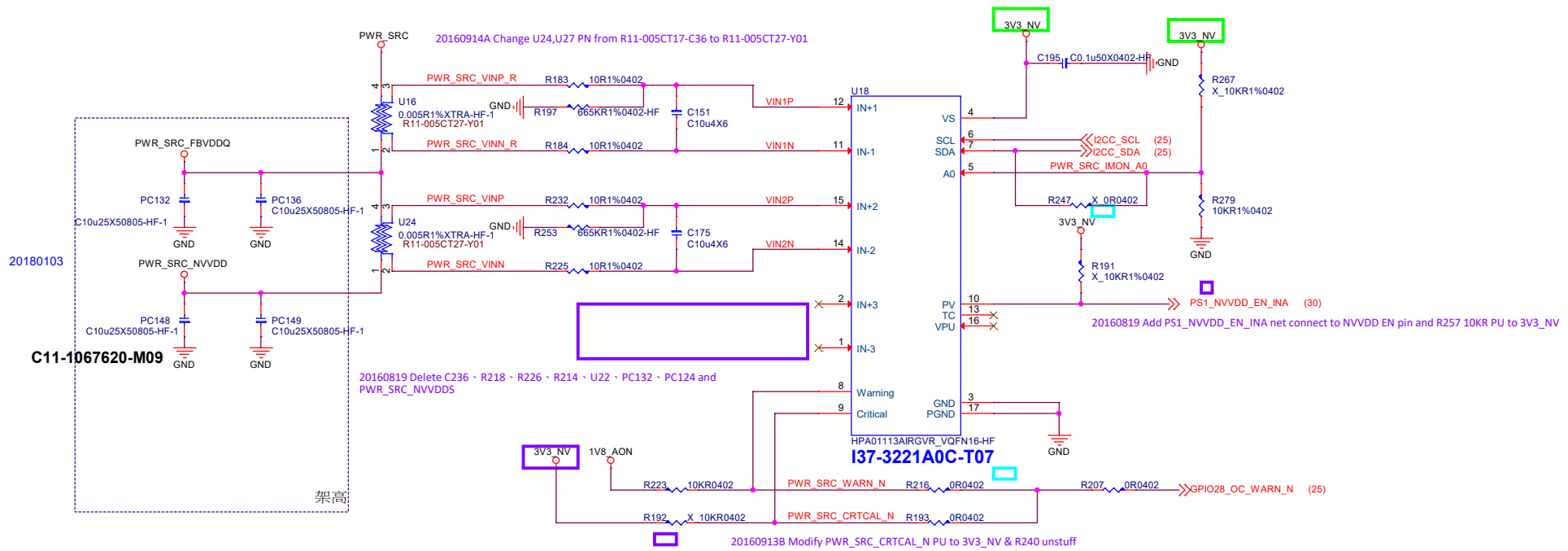
9.



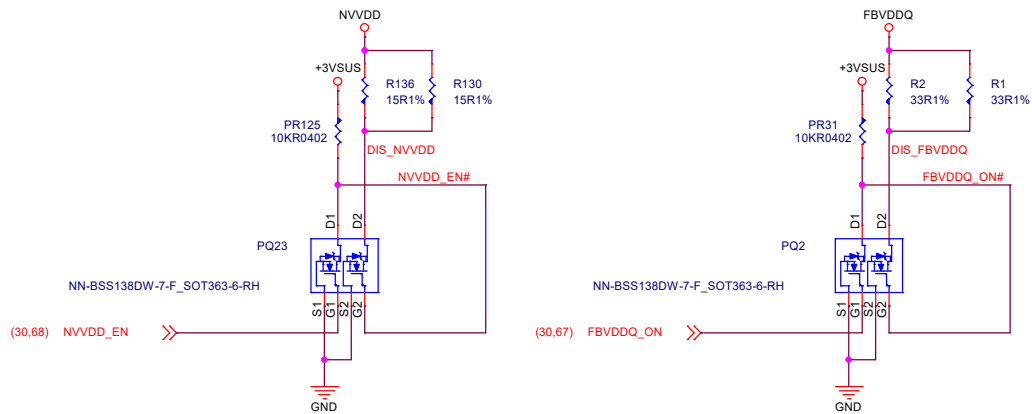
10.



DGPU_Power Control



Discharge



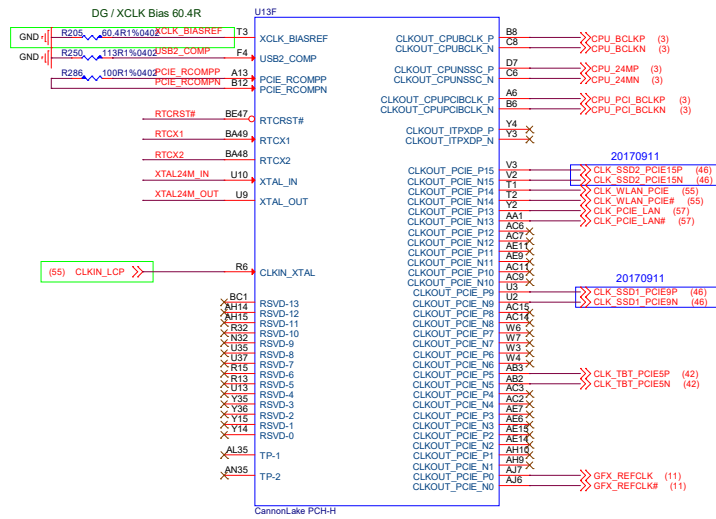
PEX_VDD 内部放電4ms

3V3_AON内部放電 2ms

1V8AON内部放電2ms

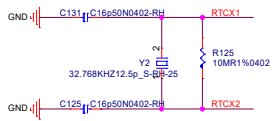
1V8_MAIN内部放電320us

HM370 (RTC/PCIE_Clock/Clock/RSVD)



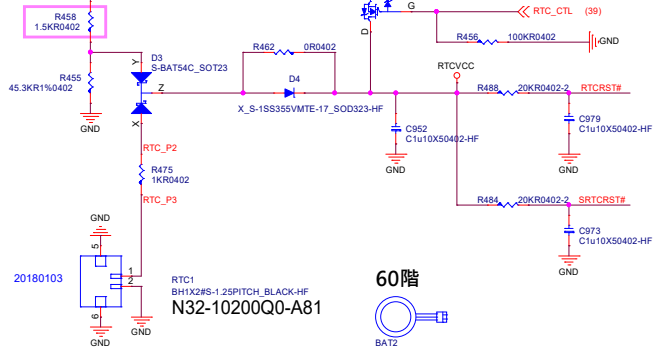
20170828 R2175 change to 200K
to follow DG and CRB

RTC Block(Close to PCH)



20170731 change R2185 to 1.5K to follow DG

RTCVCC

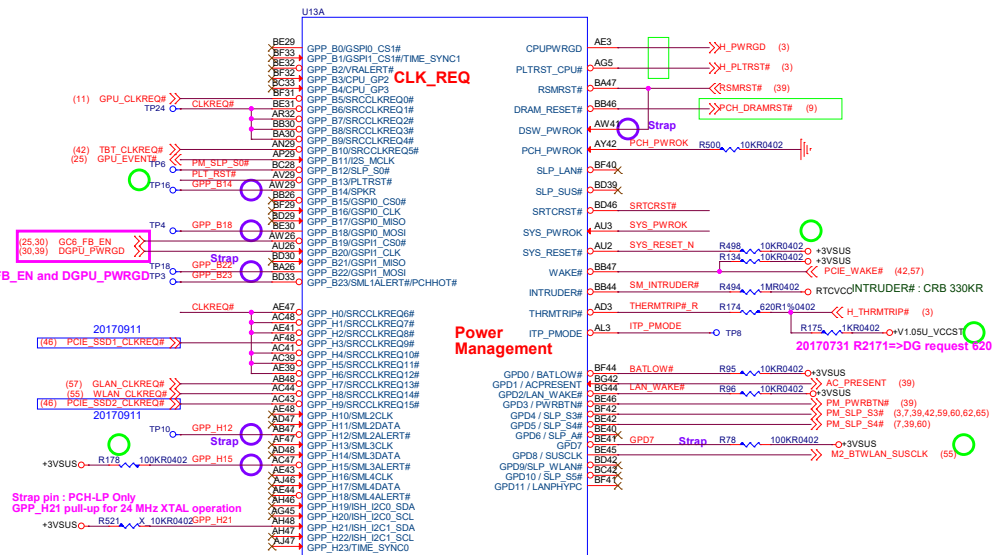


60階

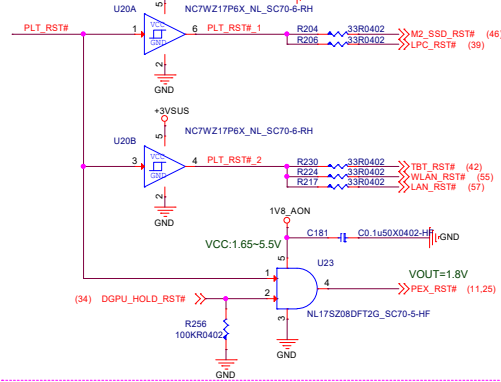


BAT2
BCR1220H2.8AM1ZB
D06-0105701-K26

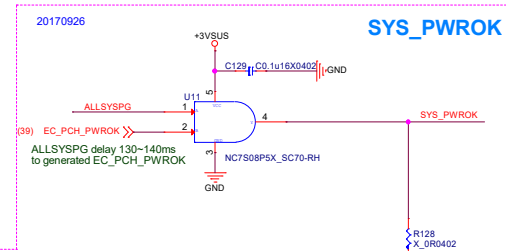
HM370 (CLKREQ/ACPI)



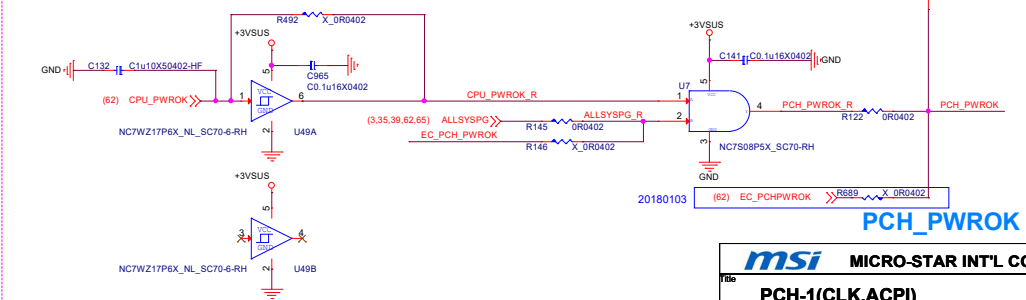
PLT_RST#



SYS_PWROK



PCH_PWROK



Functional Strap Definitions

SPKR / GPP_B14

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)

GSPI0_MOSI / GPP_B18

The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

GSP11_MOSI / GPP_B22

This Signal has a weak internal pull-down	
Bit 6 Boot BIOS	Destination
0	SPI (Default)
1	LPC

SML1ALERT# / PCHHOT#/ GPP_B23

This signal has an internal pull-down.

GPP_H12

This signal has a weak internal pull-down

GPP_H15

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

GPPD7

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be
any on-board device driving it to opposite direction
during strap sampling

DG/ RTC Well Input Strap

RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)

Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe #5				PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16	PCIe #17	PCIe #18	PCIe #19	PCIe #20	PCIe #21	PCIe #22	PCIe #23	PCIe #24	
							PCIe #1	PCIe #2	PCIe #3	PCIe #4		GBE			GBE		SATA 0a	SATA 1a	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5							
Intel® RST Support							No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

SKU	¹ SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.																													
HM370	USB3.1 Gen1 Lane 0	USB3.1 Gen1 Lane 1	USB3.1 Gen1 Lane 2	USB3.1 Gen1 Lane 3	USB3.1 Gen1 Lane 4	USB3.1 Gen1 Lane 5	USB3.1 Gen1 Lane 6	USB3.1 Gen1 Lane 7	USB3.1 Gen1 Lane 8	N/A	N/A	LAN On/Off	N/A	N/A	N/A	PCIe LAN	PCIe PCIE	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe PCIE	PCIe PCIE	PCIe SATA	PCIe SATA	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe PCIE
QM370	USB3.1 Gen1 Lane 0	USB3.1 Gen1 Lane 1	USB3.1 Gen1 Lane 2	USB3.1 Gen1 Lane 3	USB3.1 Gen1 Lane 4	USB3.1 Gen1 Lane 5	USB3.1 Gen1 Lane 6	USB3.1 Gen1 Lane 7	USB3.1 Gen1 Lane 8	USB3.1 Gen1 Lane 9	USB3.1 Gen1 Lane 10	USB3.1 Gen1 Lane 11	LAN	PCIe	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe PCIE	PCIe PCIE	PCIe SATA	PCIe SATA	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe PCIE
CM246	USB3.1 Gen1 Lane 0	USB3.1 Gen1 Lane 1	USB3.1 Gen1 Lane 2	USB3.1 Gen1 Lane 3	USB3.1 Gen1 Lane 4	USB3.1 Gen1 Lane 5	USB3.1 Gen1 Lane 6	USB3.1 Gen1 Lane 7	USB3.1 Gen1 Lane 8	USB3.1 Gen1 Lane 9	USB3.1 Gen1 Lane 10	USB3.1 Gen1 Lane 11	PCIe	LAN	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe PCIE	PCIe PCIE	PCIe SATA	PCIe SATA	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe PCIE	PCIe PCIE

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

PCIE 9-12(M2)

USB 3.1 CNT-2 USB 3.1 CNT-1

USB 3.1 CNT-3

Ref DG Section 18.6
- use Port 14 with CNVi Solution

BT

Webcam

Fingerprint

Multi-Color KB

USB 3.1 CNT-2

USB 3.1 CNT-3

USB 3.1 CNT-1

USB 2.0

USB 3.1

CNVi

CannonLake PCH-H

Intel® RST for
PCIe Storage
port
configurable
as x2/x4 M.2.

msi MICRO-STAR INT'L CO.,LTD.	
Title	
PCH-2(DMI/PCIE/USB)	
Size	Document Number
MS-16Q2	Rev 10
Date: Thursday, January 25, 2018	
Sheet	33 of 73

U13C



PCH-3(SATA/PCIE/USB OC/DDI)

ev

10

Sheet 34 of 73

Functional Strap Definitions

SMBALERT# / GPP_C2

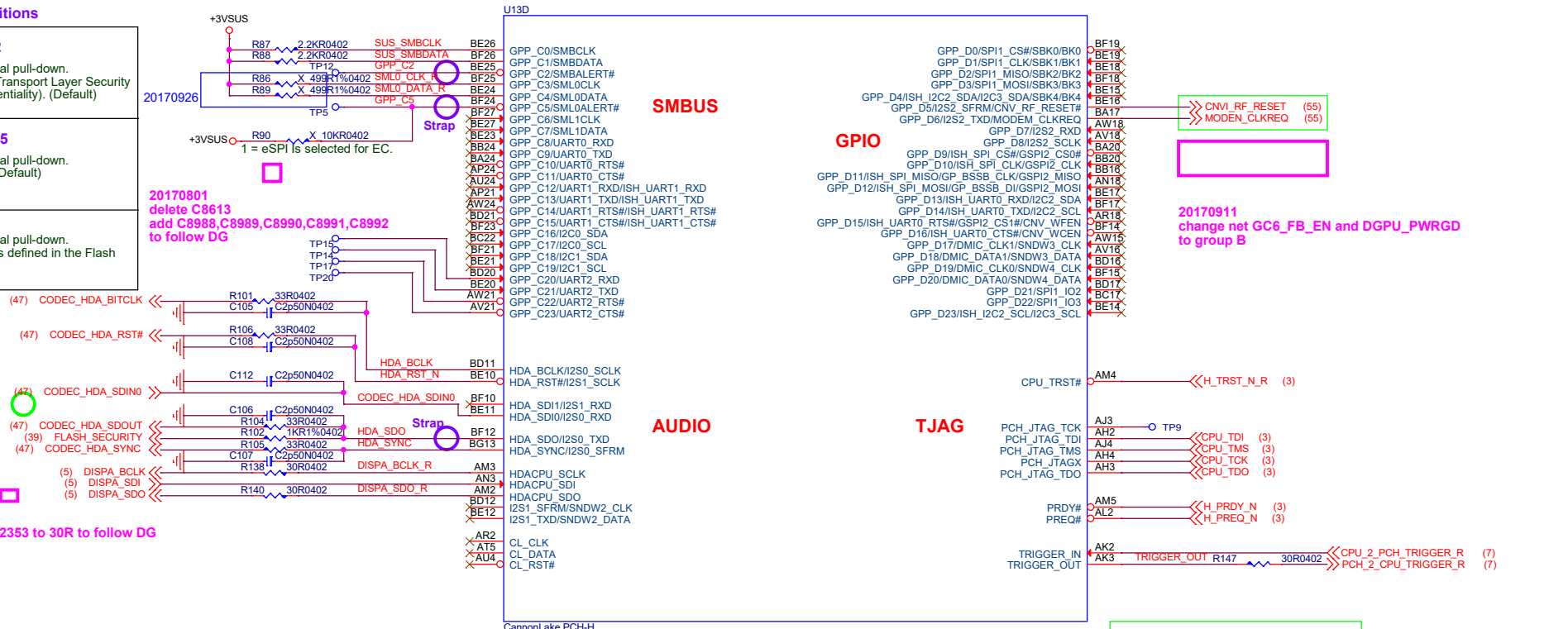
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

SML0ALERT# / GPP_C5

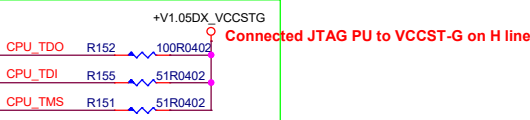
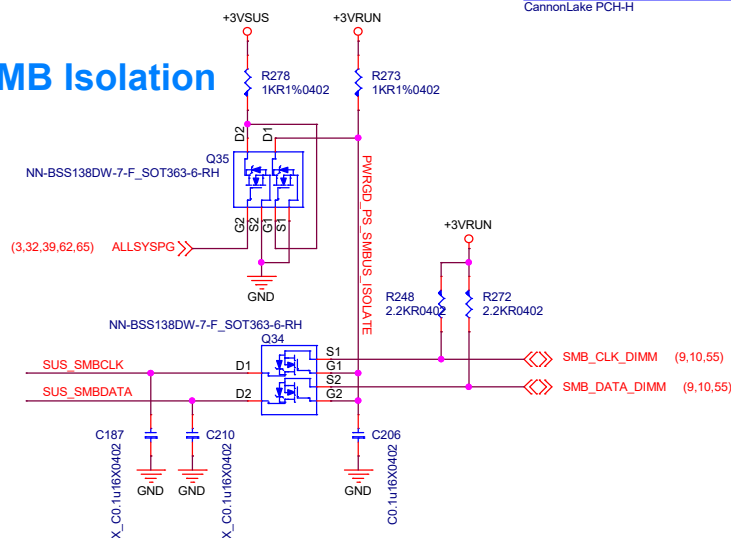
This signal has a weak internal pull-down.
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.

HDA_SDO

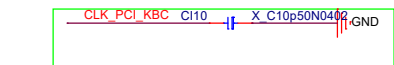
This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)



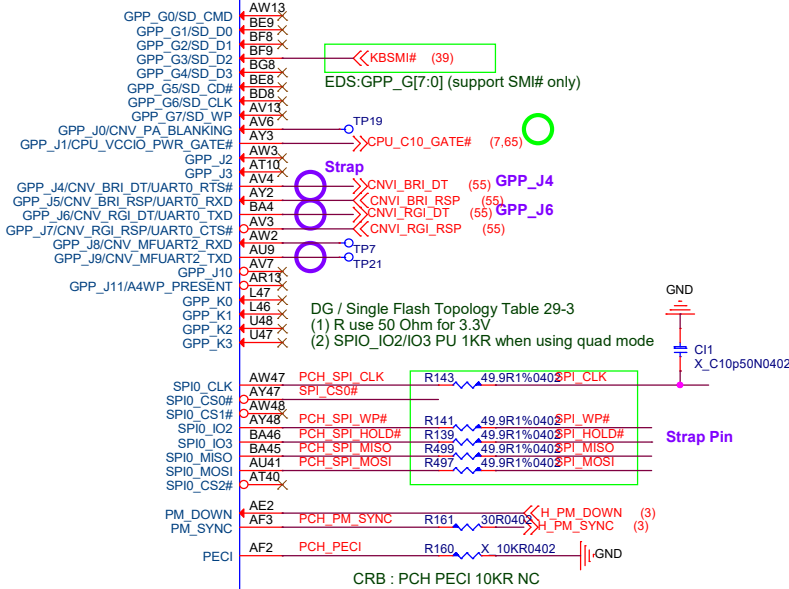
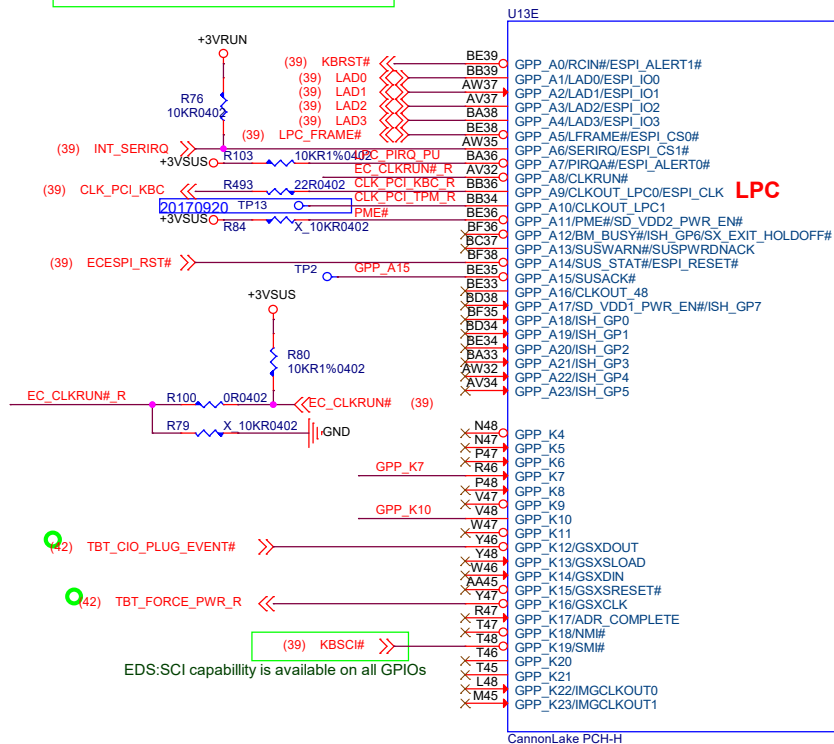
SMB Isolation



20170731 change R2226 unstuff to gollow CRB



HM370 (UART/I2C/SPI)



Functional Strap Definitions

GPP_J4

This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 Mhz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected.

GPP_J6

An external pull-up or pull-down is required. 0 = Integrated CNV/i enable. 1 = Integrated CNV/i disable.

GPP_J9

The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail

SPI0_I02

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_I03

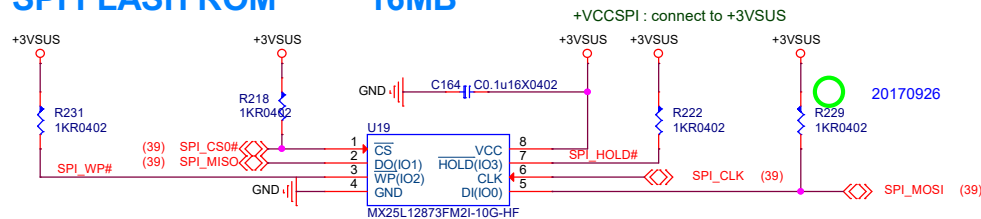
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_MOSI

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

MISO isn't Strap

SPI FLASH ROM 16MB



20170809 U79 change from socket to ROM
P/N : M31-2512832-M24

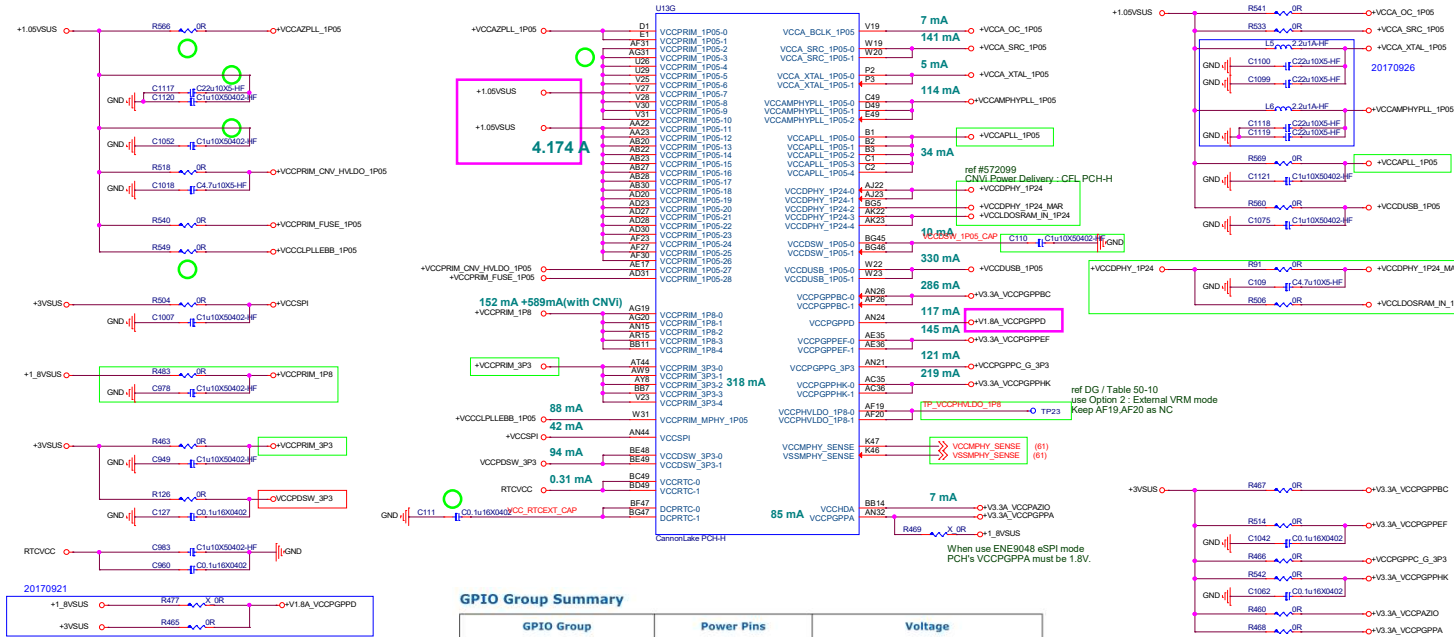
M31-2512893-W03
M-IC FLASH,128M(16Mx8bit),10ms,SOIC-8pin(208mil),WINBOND/W25Q128JVSQ,2.7V,3.6V,SPI,,HALOGEN FREE

M31-2512832-M24
M-IC FLASH,128M(16Mx8bit),40ms,SOP-8pin,MXICMX25L12873FM2I-10G(T),2.7V,3.6V,SPI,,HALOGEN FREE

msi MICRO-STAR INT'L CO.,LTD.			
Title			
PCH-5(UART/I2C/SPI)			
Size	Document Number	Rev	
	MS-16Q2	10	
Date:	Thursday, January 25, 2018	Sheet	36 of 73

HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements



GPIO Group Summary

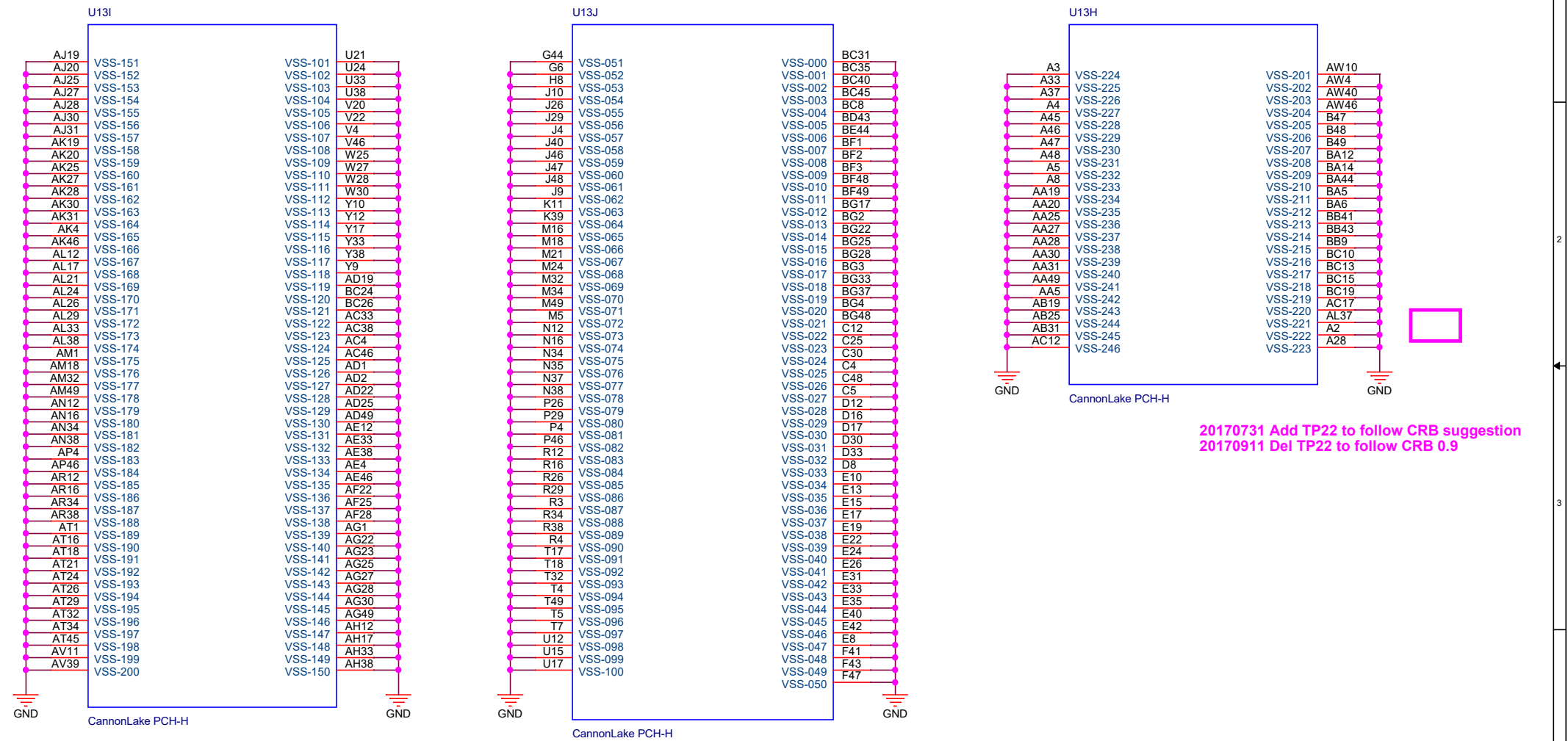
GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPBC	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPD	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

Power Descriptions for PCH in CNL-H

Name	Description
VCCA_BCLK_1P05	Analog supply for BCLK circuitries: 1.05V
VCCA_SRC_1P05	Analog supply for PCIe clock circuitries: 1.05V
VCCA_XTAL_1P05	Analog supply for XTAL circuitries: 1.05V
VCCDUSB_1P05	Supply for USB digital logic: 1.05V
VCCAPLL_1P05	Analog supply for BCLK/DMI/Audio PLLs: 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P05	Primary Well: 1.05V. For PCIe/USB3/SATA MPHY logic, I/O blocks, SRAM, JTAG, CNVI.
VCCDSW_1P05	Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P05	Mod PHY Primary: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB PLL dividers.
VCCAMPHYPLL_1P05	Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_1P8	1.8V Primary Well.
VCCPRIM_3P3	3.3V Primary Well.
VCCSPI	SPI Primary Well 3.3V or 1.8V, for SPI interface.
VCCCHDA	HDA Audio Power 3.3V, 1.8V, or 1.5V, for Intel® High Definition Audio.
VCCDSW_3P3	3.3V Deep Sx Well.
VCCRTC	RTC Well Supply. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. Note: VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. Note: Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
DCPRTC	RTC decoupling capacitor only. This rail should NOT be driven.
VCCDPHY_1P24	1.24V for CNVI logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPVLDO_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	1.8V or 3.3V for GPP_A group.
VCCPGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCPGPPD	1.8V or 3.3V for GPP_D group.
VCCPGPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCPGPPG_3P3	3.3V for GPP_G group.
VCCPGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.

PCH-H(GND)



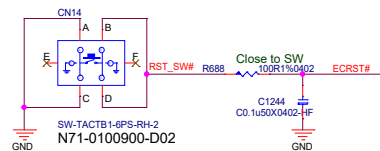
KBC/EC/uP (ENE9028)

ENE9028 & 9048 Power Notes :

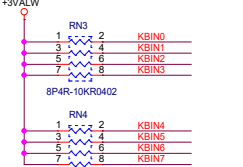
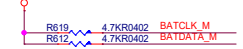
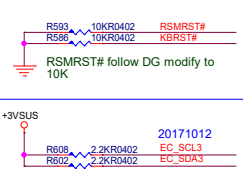
pin9 VCCLPC :
3.3V for ENE9028's LPC mode.
1.8V for ENE9048's eSPI mode.

pin111 VCC0 :
3.3V for ENE9028's PLC function
3.3V for ENE9048's eSPI operation with Pre-Driver.

Hardware Reset

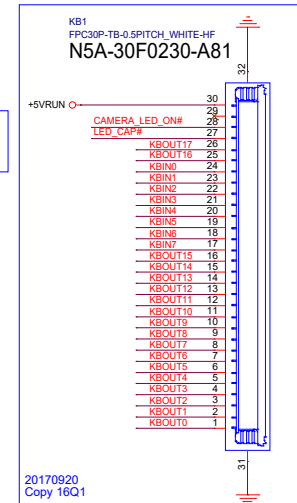
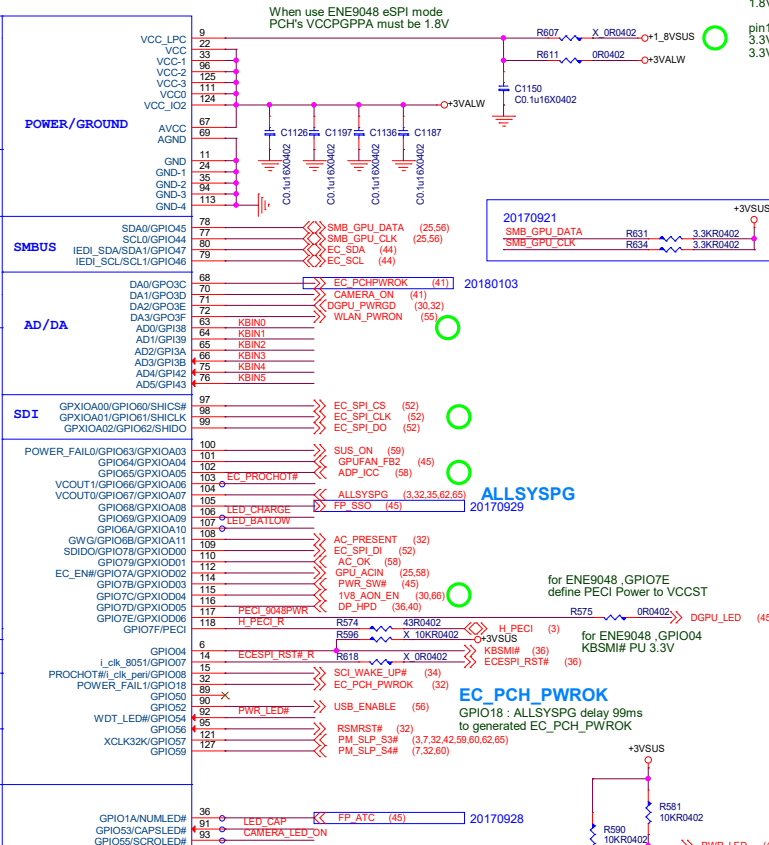
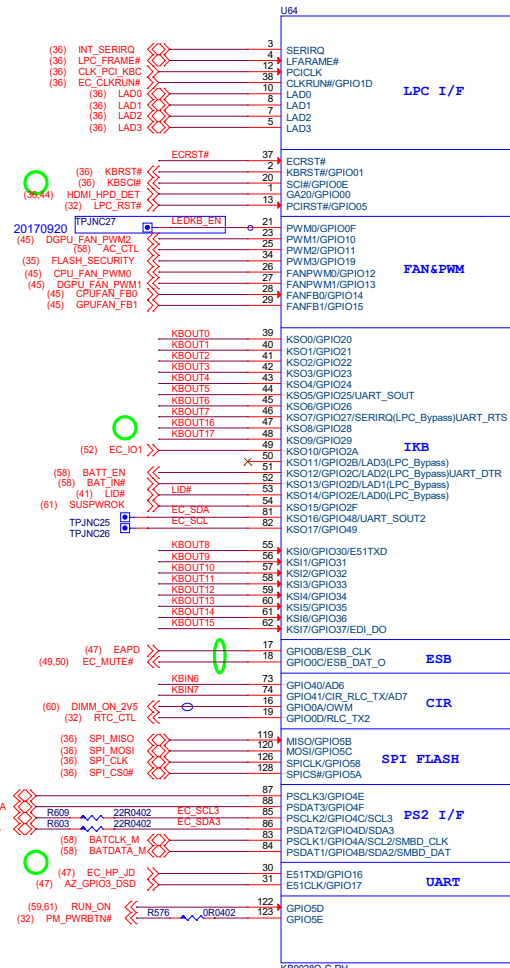
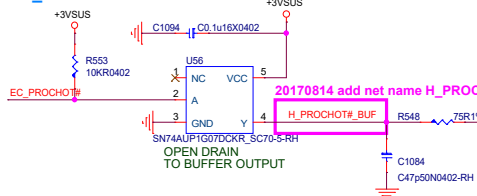


PU/PD

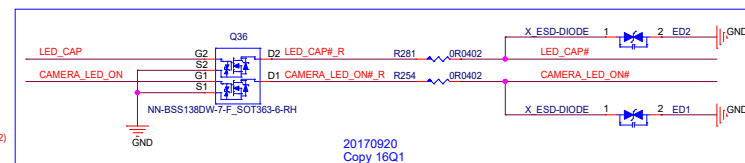
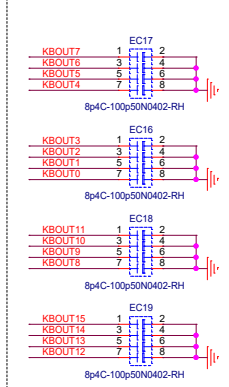


20170829 add R3528

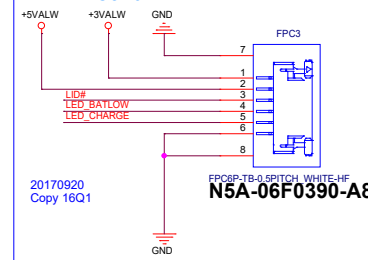
EC_PROCHOT#




For EMI



LED Board

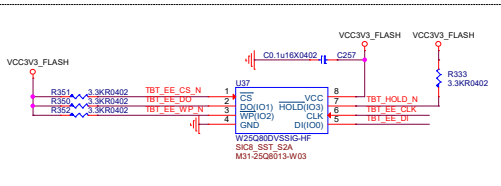


31	 MICRO-STAR INT'L CO.,LTD.	
	Title KBC/EC/uP (ENE9028)	
	Size Custom	Document Number MS-16Q2
Date: <u>September 26, 2018</u>		

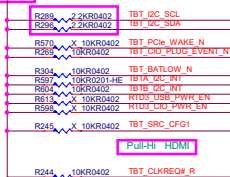
DDI C
DP++

CPUDPC_TXP1 C17
CPUDPC_TXN1 C17

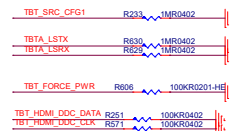
CPUDPC_TXP2 C17
CPUDPC_TXN2 C17



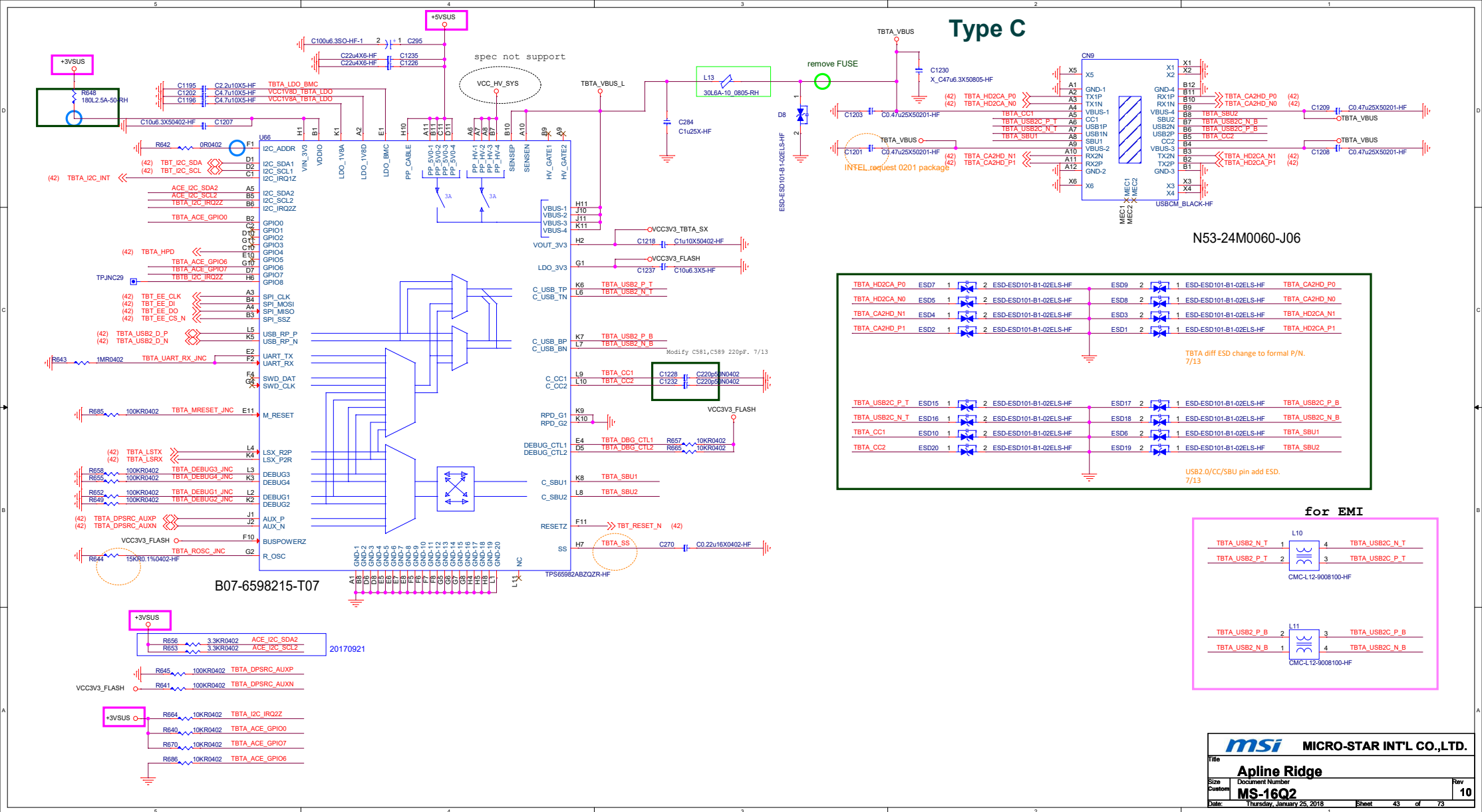
20170830
R228,R232 change to 2.2K to follow CRE



20170919
R461 change to connect with TBT_CLKREQ#_R

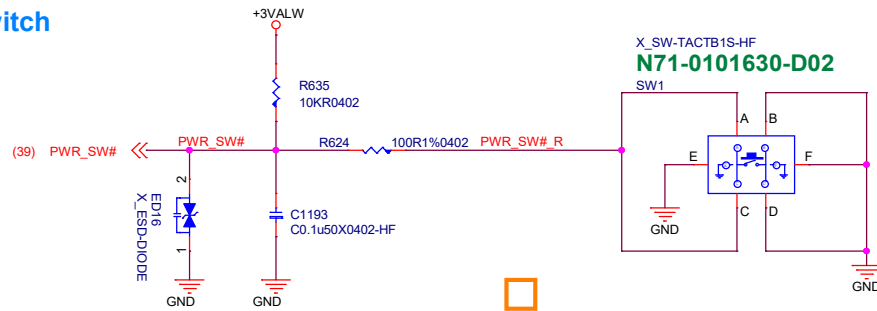
20170830
R262 change to unstuff

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100K PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_S1
POC_GPIO_1	10K PU	VCC3V3_TBT_S1
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_S1
POC_GPIO_5	10K PU	VCC3V3_TBT_S1

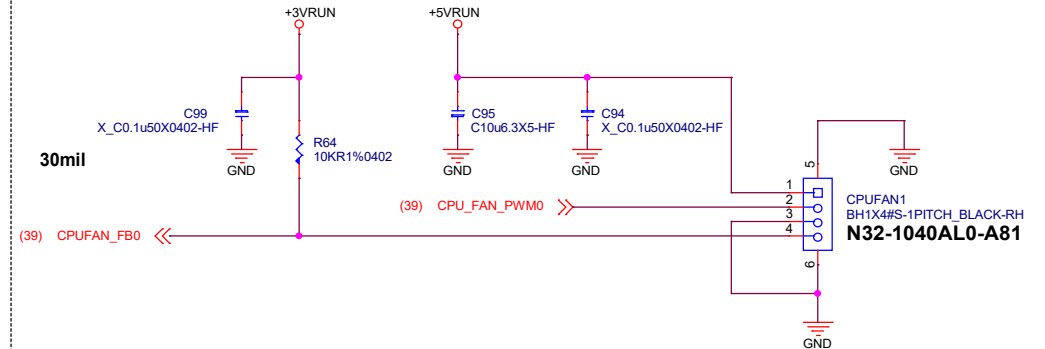


PWR SW/CPU FAN/BTB CONN/ LED CONN

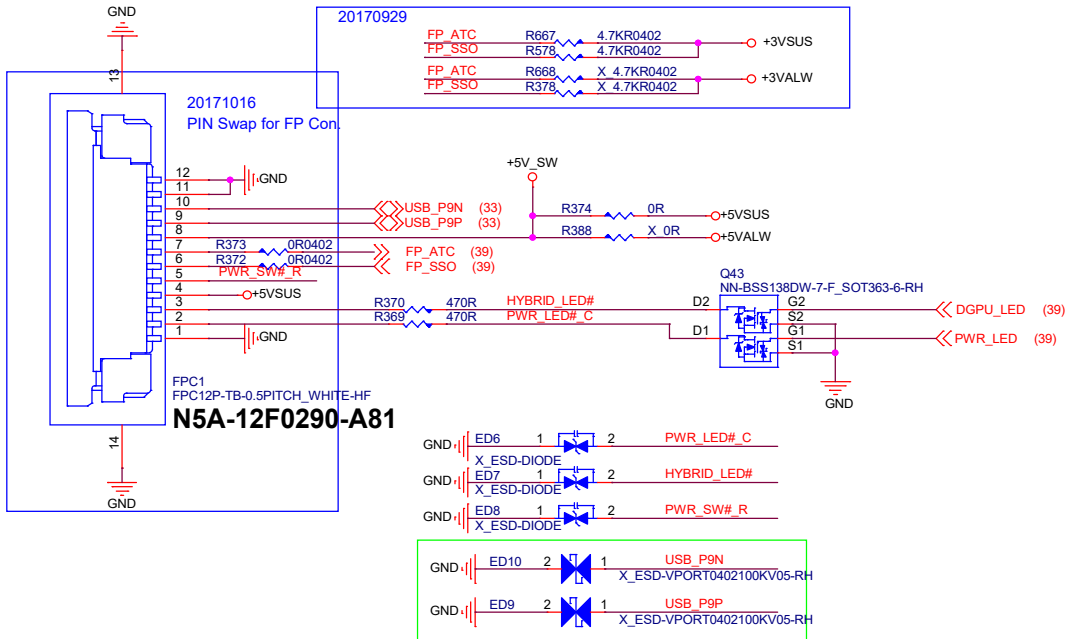
Power Switch



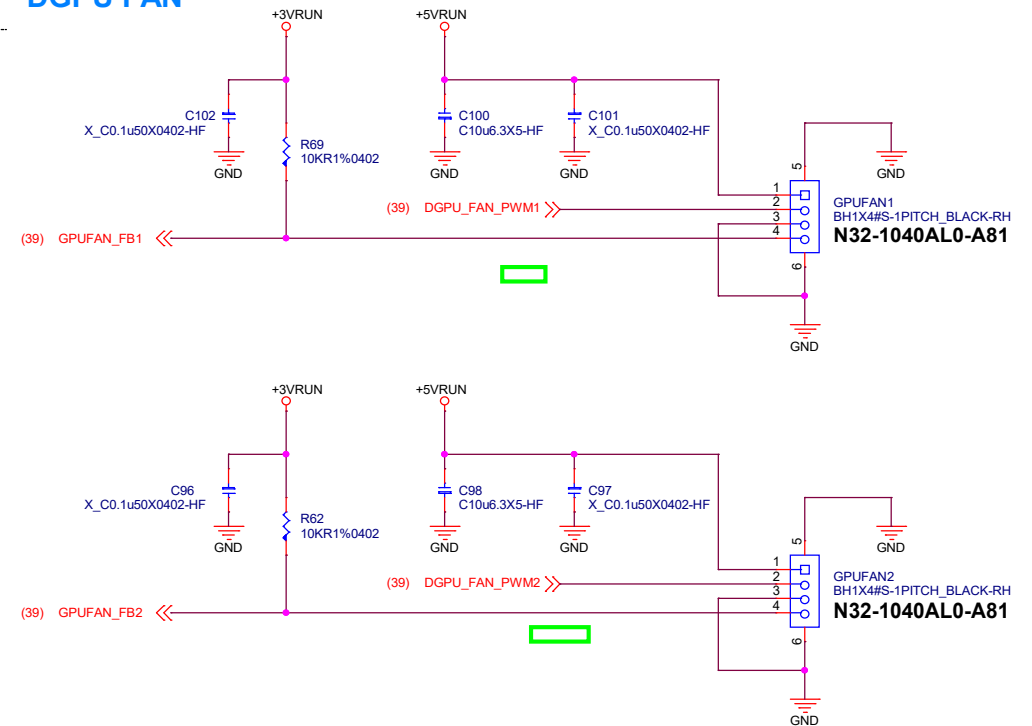
CPU FAN



Power LED+SW+FP



DGPU FAN



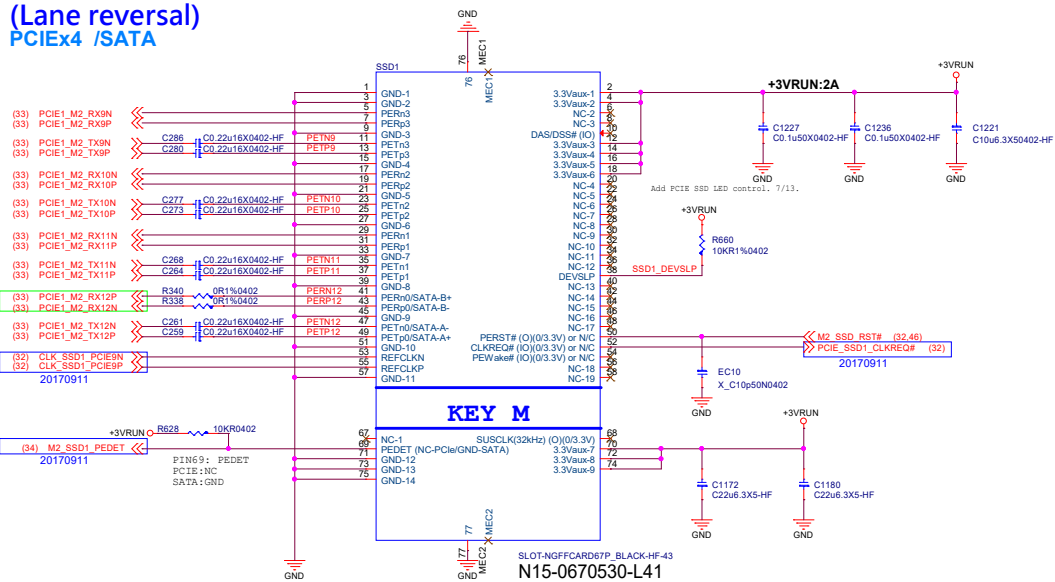
msi MICRO-STAR INT'L CO.,LTD.

Title			CPU FAN/LED/PWR SW
Size	Document Number	Rev	10
Custom	MS-16Q2		
Date:	Thursday, January 25, 2018	Sheet	45 of 73

M2 SSD -1

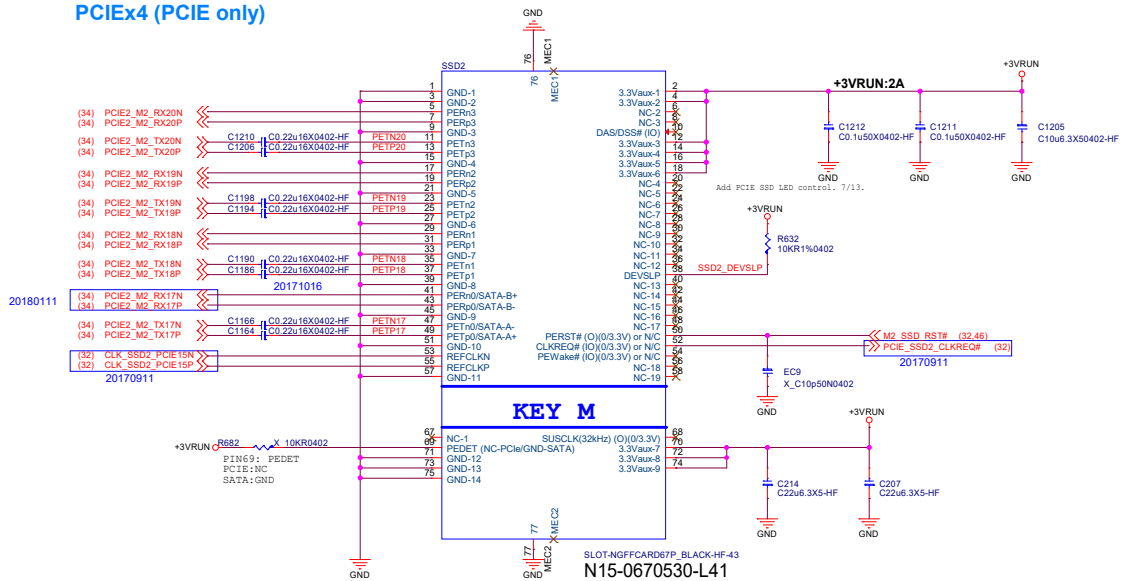
(Lane reversal)

PCIEx4 /SATA



M2 SSD -2

PCIEx4 (PCIe only)



AUDIO(ALC1220)

ALC1220	AZ_GPIO3_DSD
PCM	H
DSD	L

To EC
To EC

Internal Mic

To EC

DIGITAL

Analog

To Mux

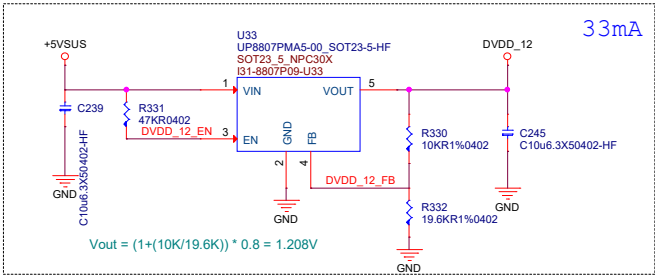
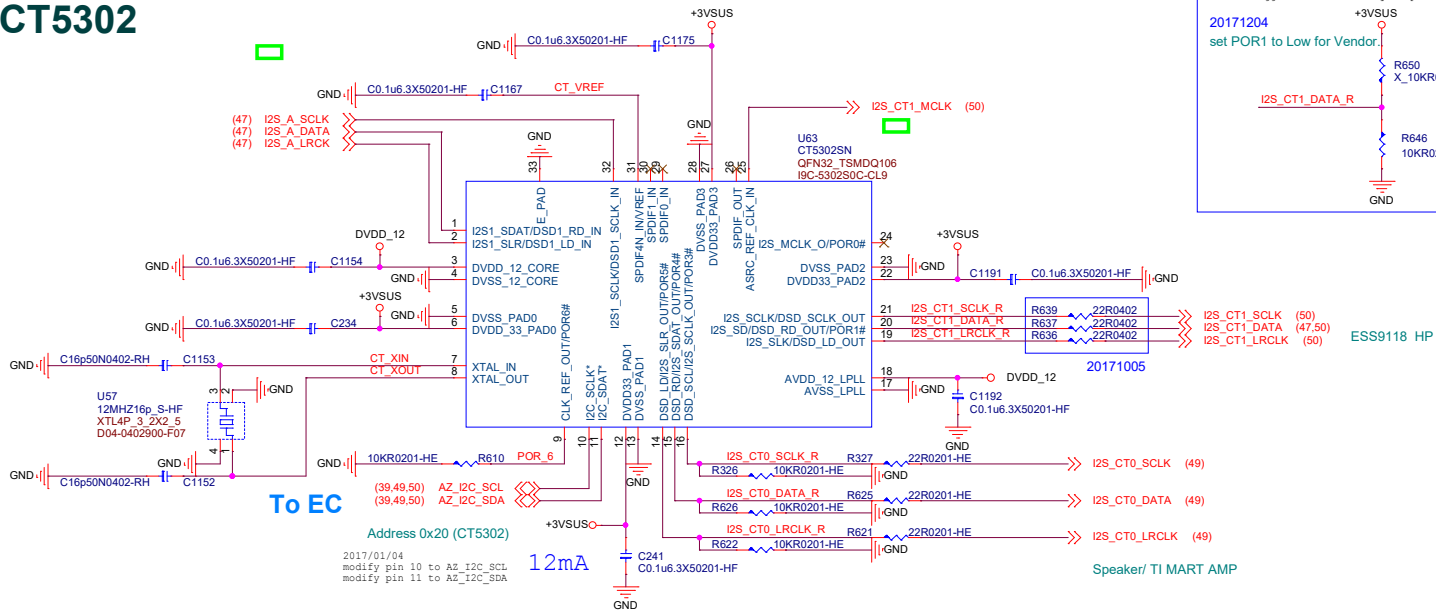
MIC In

EMI
Close Codec

20170809 EMI remove C8176

msi MICRO-STAR INT'L CO.,LTD.			
Title Audio(ALC1220)			
Size	Document Number	Rev	
Custom	MS-16Q2	10	
Date:	Thursday, January 25, 2018	Sheet	47 of 73

CT5302



Pin Name	Description	Function Table
POR_IN_1	POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	Select I2S1 output port is master or slave mode
POR_IN_3	POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	Select Crystal frequency
POR_IN_4		
POR_IN_5	POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	I2C serial interface device ID selection
POR_IN_6		

HW SETTING

HW SETTING

HW SETTING

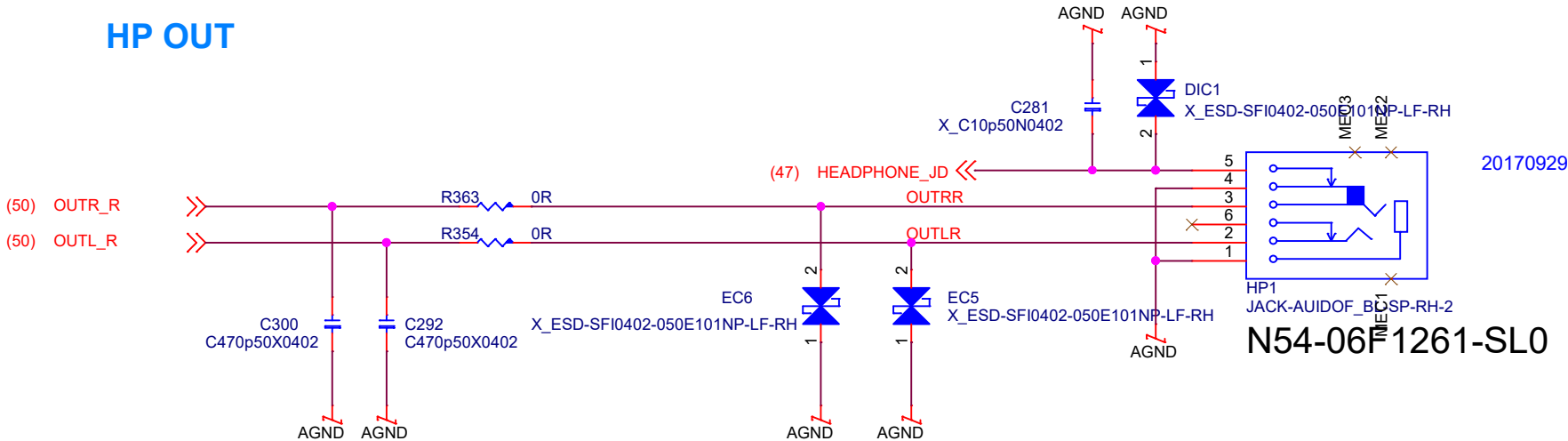
I2S output slave mode:		
Select I2S1 output port		
No.	POR1	Definition
0	0	I2S output master mode
1	1	I2S output slave mode

Hardware Crystal:			
Select current external crystal frequency			
No	POR4	POR3	Definition
0	0	0	12.0000MHz
1	0	1	11.2896MHz
2	1	0	12.2880MHz
3	1	1	14.3180MHz

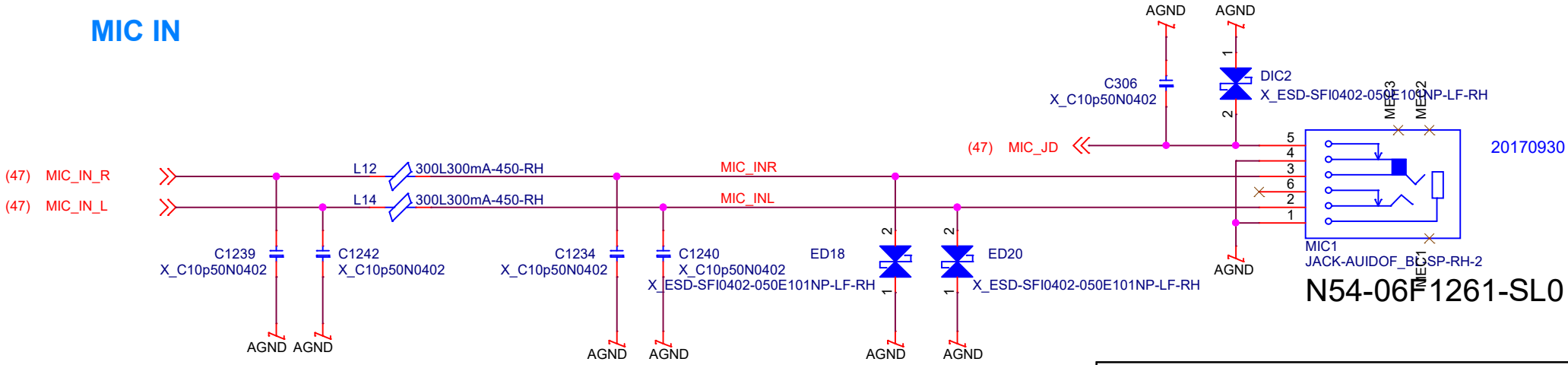
I2C Slave ID			
Define chip I2C slave address			
No	POR6	POR5	Definition
0	0	0	0x20
1	0	1	0x22
2	1	0	0x24
3	1	1	0x26


Audio CONN

HP OUT



MIC IN



		MICRO-STAR INT'L CO.,LTD.	
Title			
Audio Jack			
Size	Document Number		Rev
Custom	MS-16Q2		10
Date:	Thursday, January 25, 2018	Sheet	51 of 73

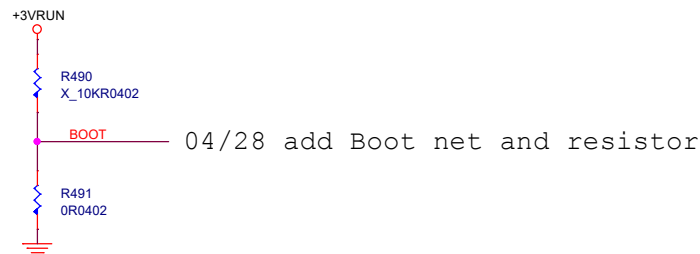
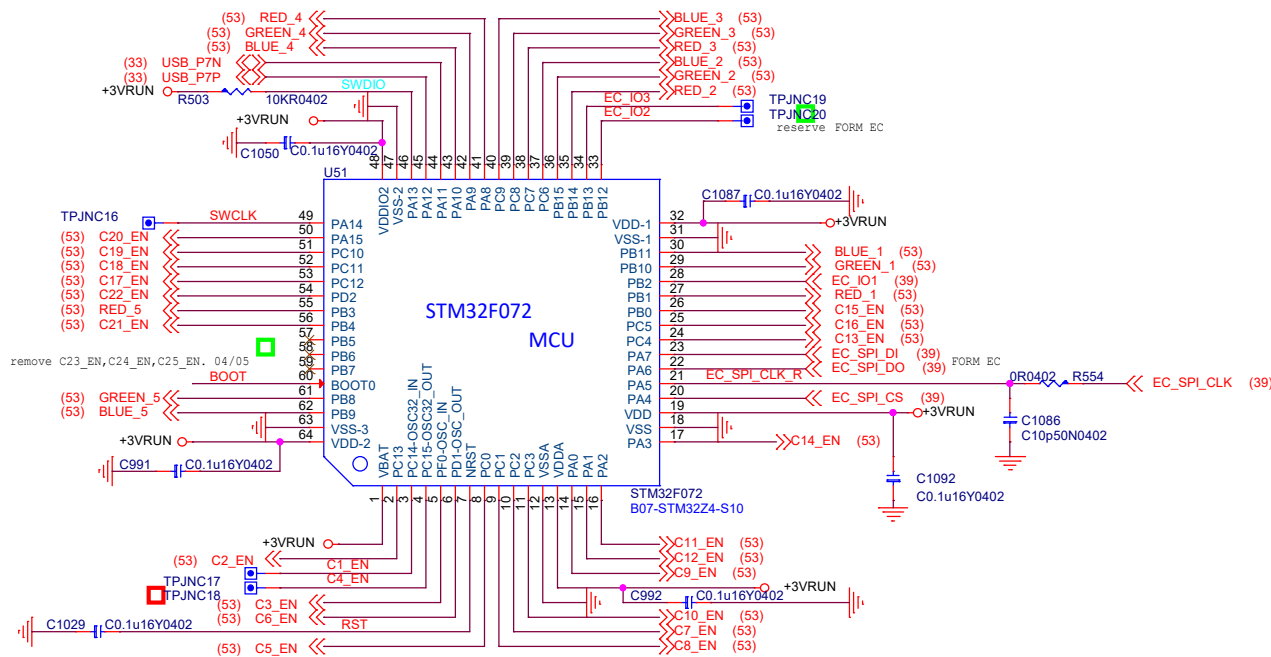
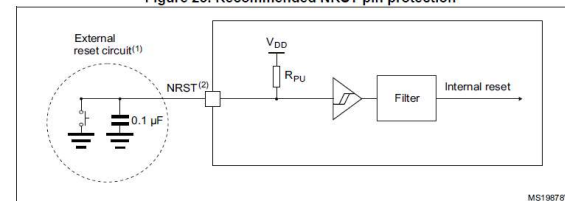
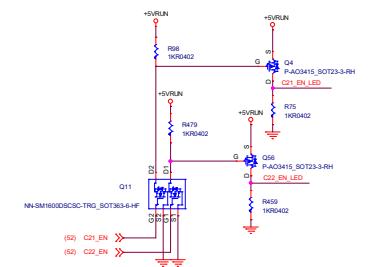


Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 56: NRST pin characteristics](#). Otherwise the reset will not be taken into account by the device.



Change C5_EN control. 2017/4/24

	PWM1	PWM2	PWM3	PWM4	PWM5
MCU_C1_EN					
MCU_C2_EN		P			F3
MCU_C3_EN			PgUp	F4	INS
MCU_C4_EN					
MCU_C5_EN		RIGHT	UP	DOWN	LEFT
MCU_C6_EN		F5	PgDn	F6	DEL
MCU_C7_EN	F8	CAP	A	S	D
MCU_C8_EN	F9	TAB	Q	W	E
MCU_C9_EN	F10	CTRL_L	WIN_L	ALT_L	K131
MCU_C10_EN	F11	SHI_L	\ (K45)	Z	X
MCU_C11_EN	V	B	N	M	<,
MCU_C12_EN	F12	SPACE	3#	K132	C
MCU_C13_EN	>.	/?	K56	SHI_R	ENT
MCU_C14_EN	K133	ALTR	SS (Fn)	2@	CTR_R
MCU_C15_EN	F	G	H	J	K
MCU_C16_EN	L	::	""	K42	\ (K29)
MCU_C17_EN	O	F7	{[}]	BACK
MCU_C18_EN	R	T	Y	U	I
MCU_C19_EN	9(0)	-_	+=	k14
MCU_C20_EN	4\$	5%	6^	7&	8*
MCU_C21_EN	`~	1!	ESC	F1	F2
MCU_C22_EN	PAUSE	SCR	PRT		
MCU_C23_EN					
MCU_C24_EN					
MCU_C25_EN					

Mapping to
KBC's KBIN & KBOUT

KBIN_3,KBOUT_9	KBIN_6,KBOUT_5	KBIN_7,KBOUT_5	KBIN_7,KBOUT_4	KBIN_6,KBOUT_9
KBIN_3,KBOUT_5		KBIN_4,KBOUT_9	KBIN_5,KBOUT_9	
KBIN_1,KBOUT_12	KBIN_2,KBOUT_5	KBIN_6,KBOUT_12	KBIN_4,KBOUT_12	KBIN_2,KBOUT_12
KBIN_2,KBOUT_9	KBIN_4,KBOUT_5	KBIN_5,KBOUT_5	KBIN_5,KBOUT_4	KBIN_7,KBOUT_9
KBIN_6,KBOUT_4	KBIN_4,KBOUT_4	KBIN_1,KBOUT_4	KBIN_2,KBOUT_4	KBIN_0,KBOUT_4
KBIN_3,KBOUT_4		KBIN_7,KBOUT_12	KBIN_5,KBOUT_12	KBIN_3,KBOUT_12
	KBIN_0,KBOUT_13	KBIN_4,KBOUT_0	KBIN_5,KBOUT_0	KBIN_4,KBOUT_1
	KBIN_1,KBOUT_3	KBIN_2,KBOUT_0	KBIN_3,KBOUT_0	KBIN_2,KBOUT_1
	KBIN_3,KBOUT_3	KBIN_7,KBOUT_13	KBIN_4,KBOUT_3	KBIN_2,KBOUT_13
	KBIN_2,KBOUT_3	KBIN_0,KBOUT_9	KBIN_6,KBOUT_0	KBIN_7,KBOUT_0
KBIN_7,KBOUT_1	KBIN_6,KBOUT_2	KBIN_7,KBOUT_2	KBIN_6,KBOUT_6	KBIN_7,KBOUT_6
	KBIN_5,KBOUT_3		KBIN_5,KBOUT_13	KBIN_6,KBOUT_1
KBIN_6,KBOUT_7	KBIN_7,KBOUT_7	KBIN_6,KBOUT_8	KBIN_7,KBOUT_8	KBIN_1,KBOUT_5
KBIN_6,KBOUT_13	KBIN_6,KBOUT_3	KBIN_1,KBOUT_13	KBIN_3,KBOUT_13	KBIN_7,KBOUT_3
KBIN_5,KBOUT_1	KBIN_4,KBOUT_2	KBIN_5,KBOUT_2	KBIN_4,KBOUT_6	KBIN_5,KBOUT_6
KBIN_4,KBOUT_7	KBIN_5,KBOUT_7	KBIN_4,KBOUT_8	KBIN_5,KBOUT_8	KBIN_0,KBOUT_5
KBIN_2,KBOUT_7		KBIN_2,KBOUT_8	KBIN_3,KBOUT_8	KBIN_0,KBOUT_12
KBIN_3,KBOUT_1	KBIN_2,KBOUT_2	KBIN_3,KBOUT_2	KBIN_2,KBOUT_6	KBIN_3,KBOUT_6
KBIN_0,KBOUT_7	KBIN_1,KBOUT_7	KBIN_0,KBOUT_8	KBIN_1,KBOUT_8	KBIN_1,KBOUT_9
KBIN_1,KBOUT_1	KBIN_0,KBOUT_2	KBIN_1,KBOUT_2	KBIN_0,KBOUT_6	KBIN_1,KBOUT_6
		KBIN_0,KBOUT_10	KBIN_1,KBOUT_10	KBIN_2,KBOUT_10
	KBIN_0,KBOUT_3	KBIN_0,KBOUT_0	KBIN_1,KBOUT_0	KBIN_0,KBOUT_1
KBIN_0,KBOUT_11	KBIN_1,KBOUT_11	KBIN_2,KBOUT_11	KBIN_3,KBOUT_11	KBIN_4,KBOUT_11
KBIN_3,KBOUT_10	KBIN_4,KBOUT_10	KBIN_5,KBOUT_10	KBIN_6,KBOUT_10	KBIN_7,KBOUT_10
KBIN_3,KBOUT_7		KBIN_7,KBOUT_11	KBIN_6,KBOUT_11	KBIN_5,KBOUT_11



msi

MICRO-STAR INT'L CO.,LTD.

Title

Keyboard Matrix

Size

Document Number

MS-16Q2

Rev

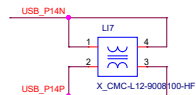
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Date:

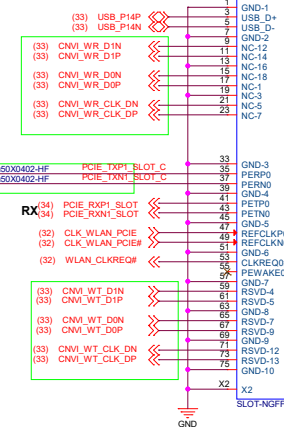
Sheet 54 of 73

WLAN /ClickPad/FP

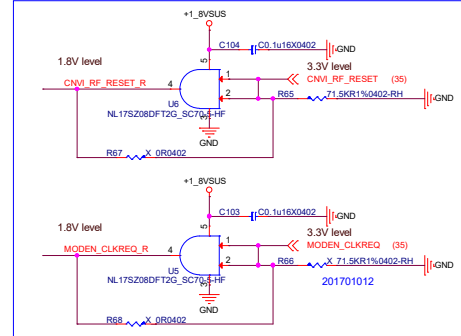
EMI



Ref DG Section 18.6
- use USB 2.0 Port 14 with CNVi Solution



N15-0670520-L41
SLOT_NGFFCARD67_H2_15



20170817 change R2394 stuff and R2397 unstuff for strap pin setting

Functional Strap Definitions

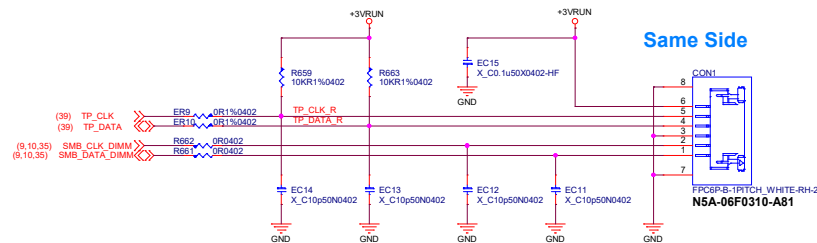
GPP_J4

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 Mhz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24Mhz XTAL frequency selected.

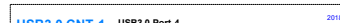
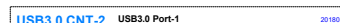
GPP_J6

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

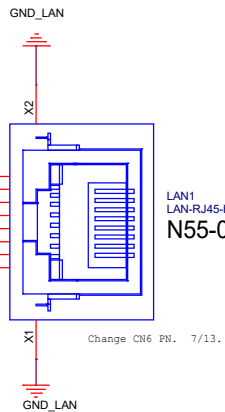
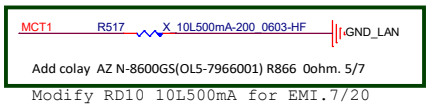
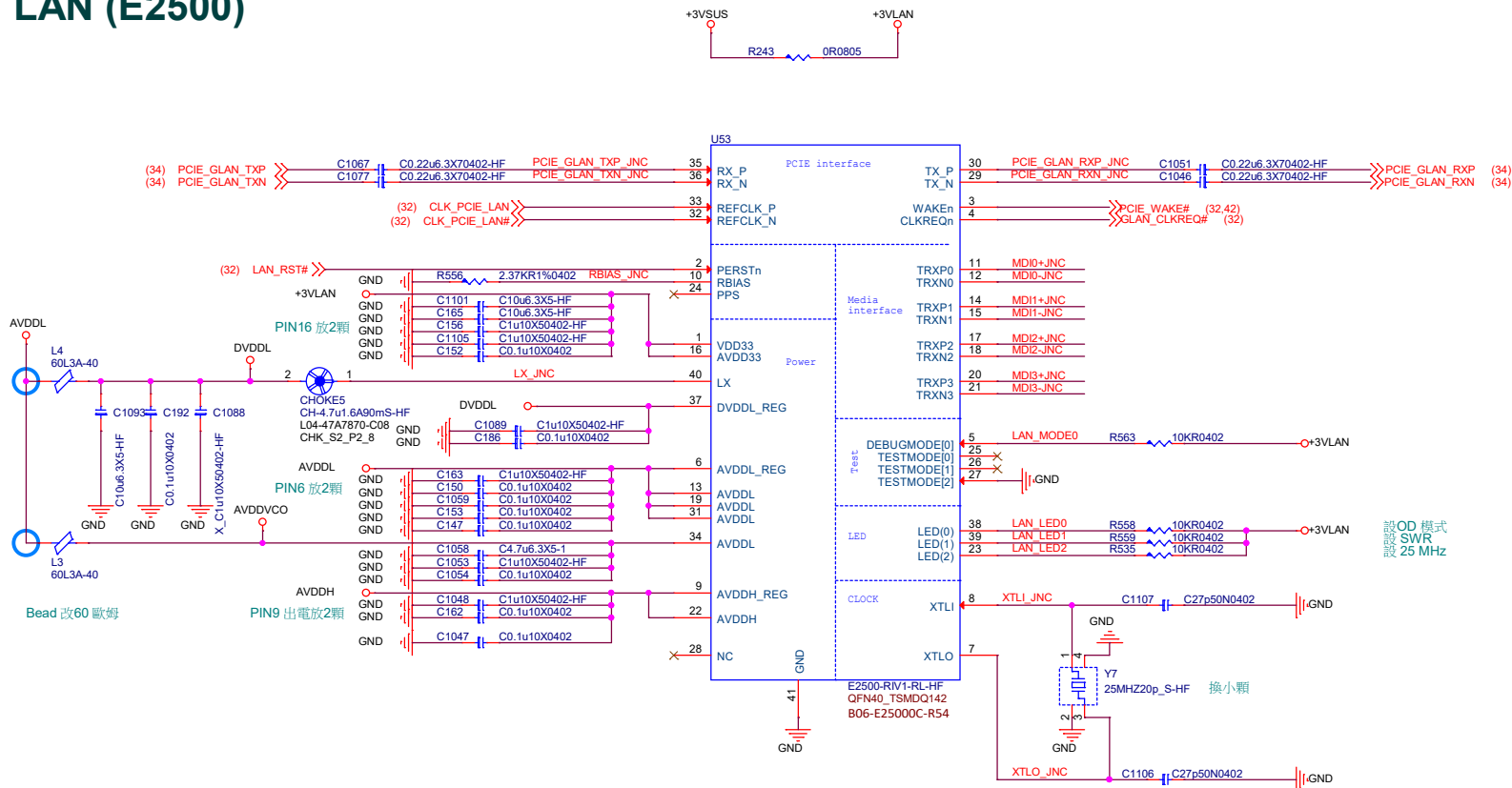
Click Pad



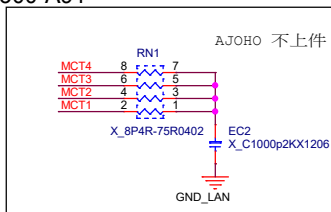
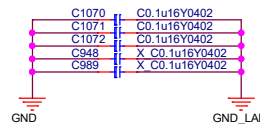
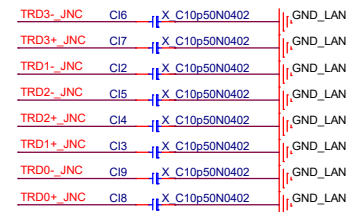
Same Side



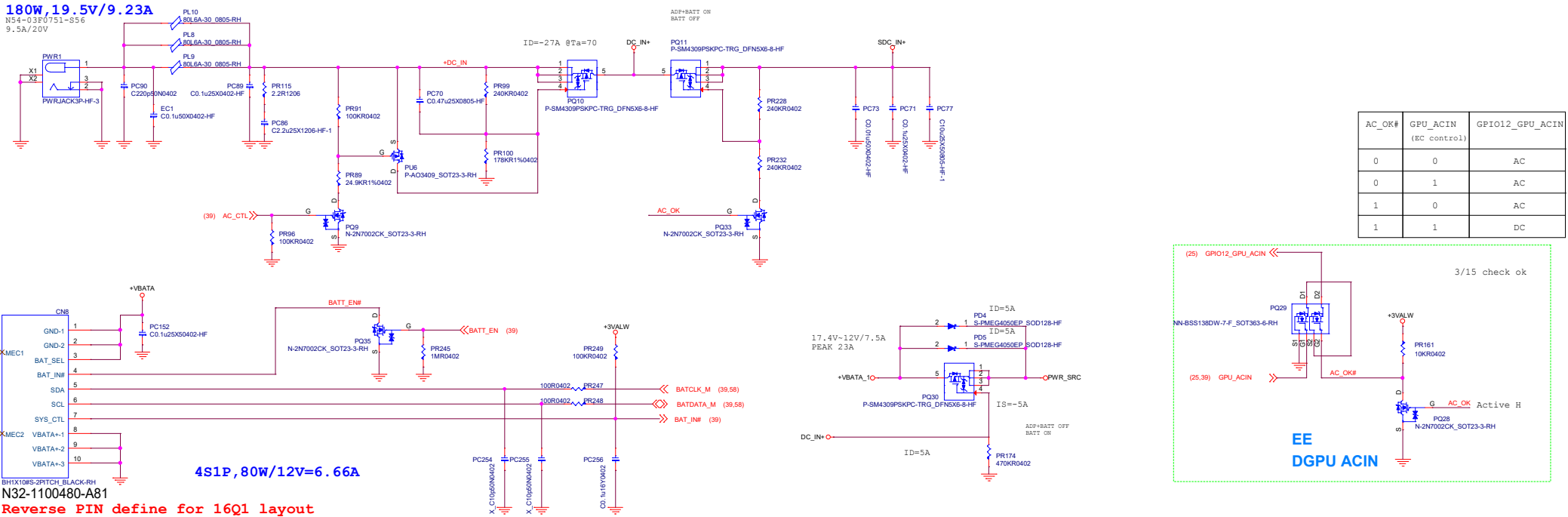
LAN (E2500)



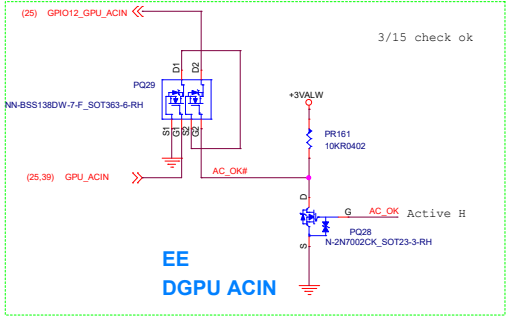
LAN1
LAN-RJ45-HF-4
N55-08F0691-AF2



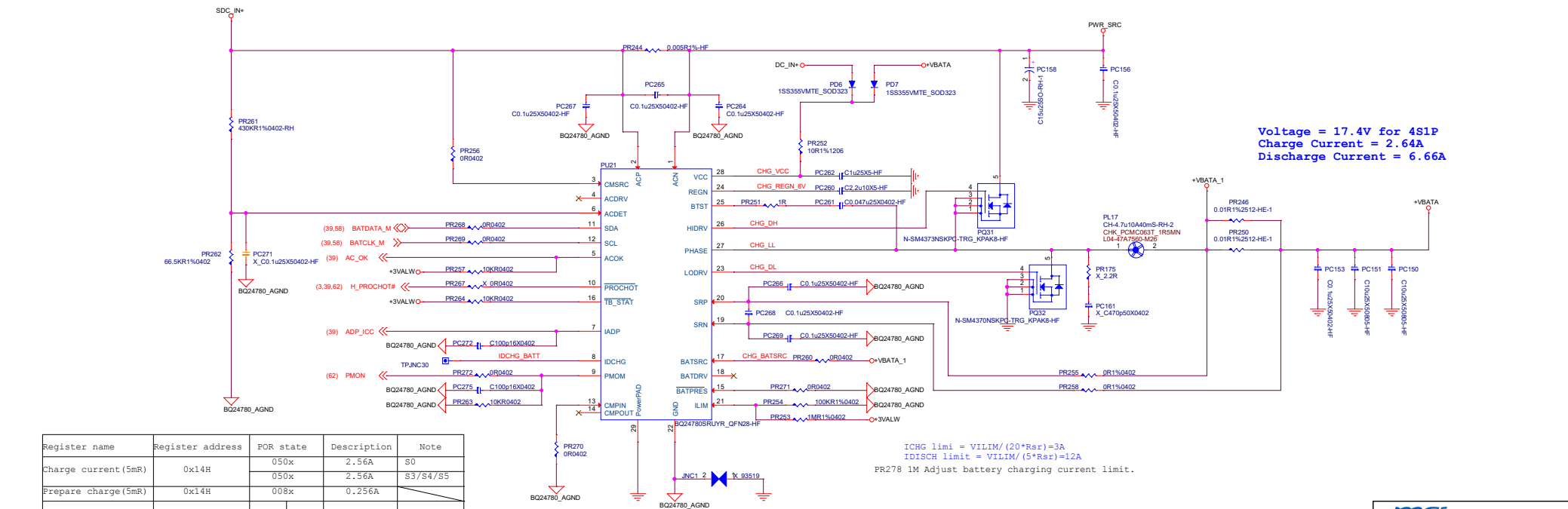
N92-03M0941-SL0
180W, 19.5V/9.23A
N54-03F0751-S56
9.5A/20V



AC_OK#	GPU_ACIN (EC control)	GPIO12_GPU_ACIN
0	0	AC
0	1	AC
1	0	AC
1	1	DC



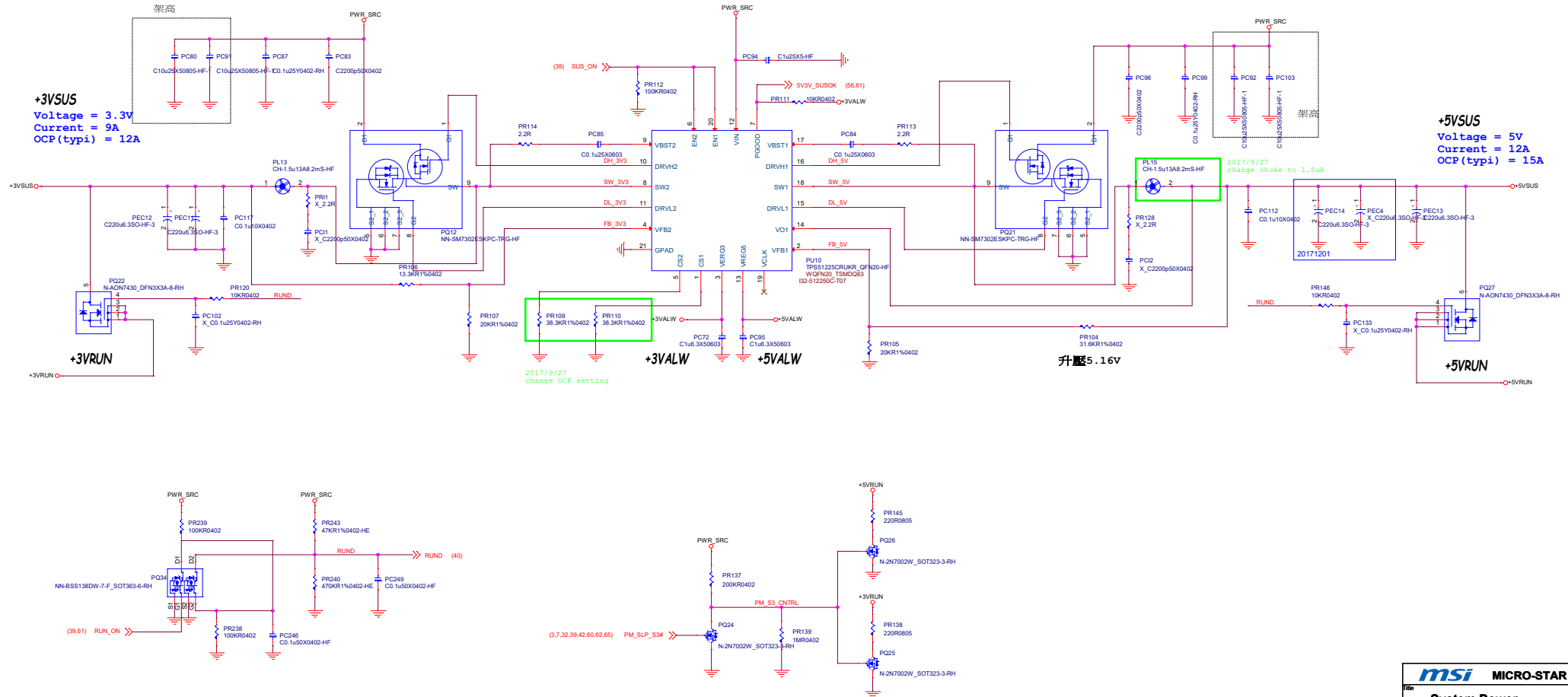
4S1P, 80W/12V=6.66A
N32-1100480-A81
Reverse PIN define for 16Q1 layout



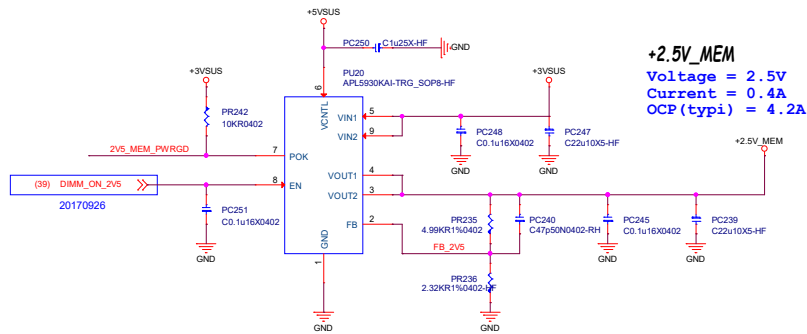
Voltage = 17.4V for 4S1P
Charge Current = 2.64A
Discharge Current = 6.66A

Register name	Register address	POR state	Description	Note
Charge current(5mR)	0x14H	050x	2.56A	S0
Prepare charge(5mR)	0x14H	008x	0.256A	S3/S4/S5
Input current(5mR)	0x3FH	19.5V 110x	8.704A	180W
Charge voltage	0x15H	43Fx	17.392V	4S1P
Discharge current(5mR)	0x39H	080x	4.096A	BOOST current

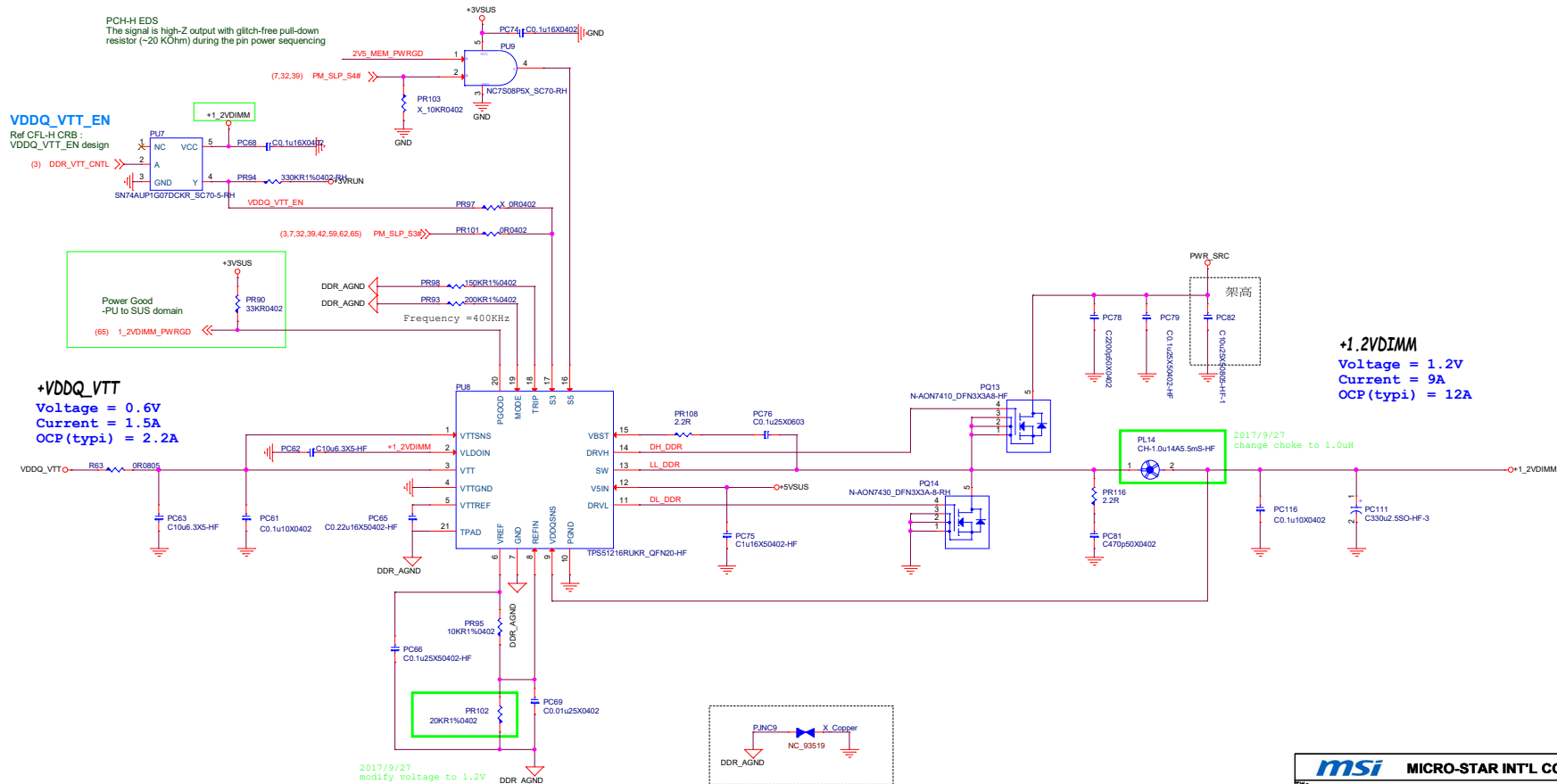
System Power



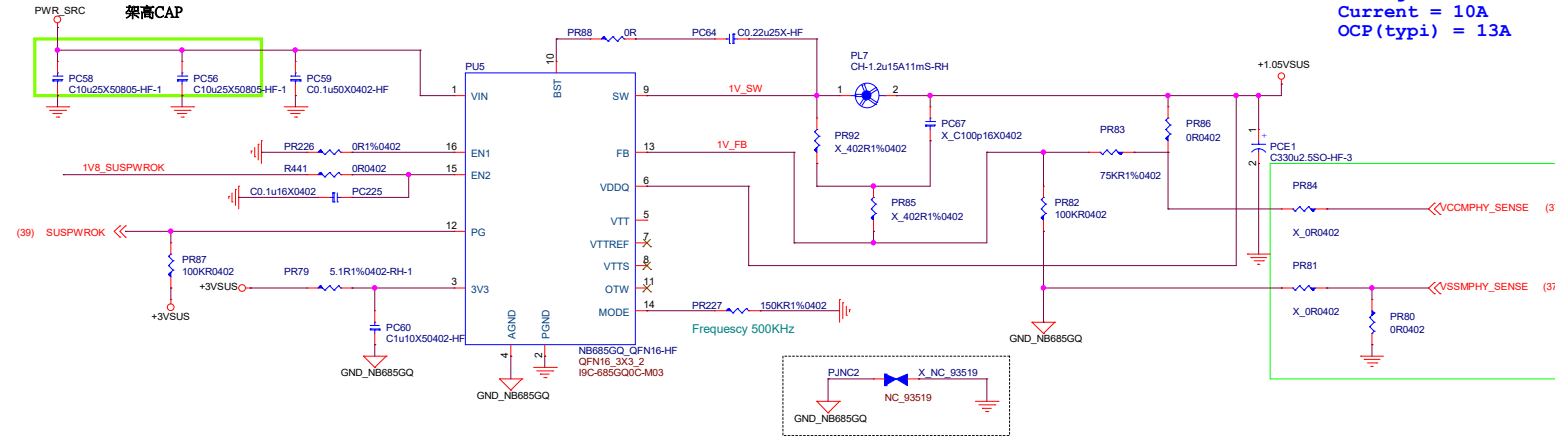
+2.5V_MEM (DDR4/Vpp)



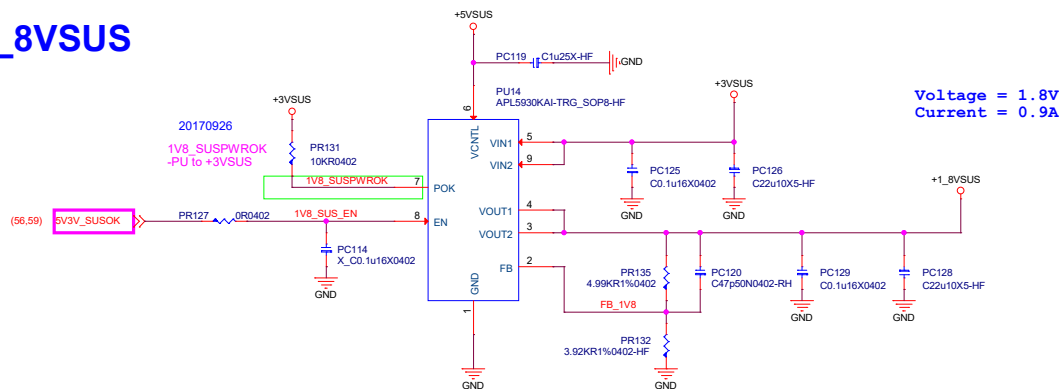
+1.2VDIMM / VDDQ_VTT(0.6V)



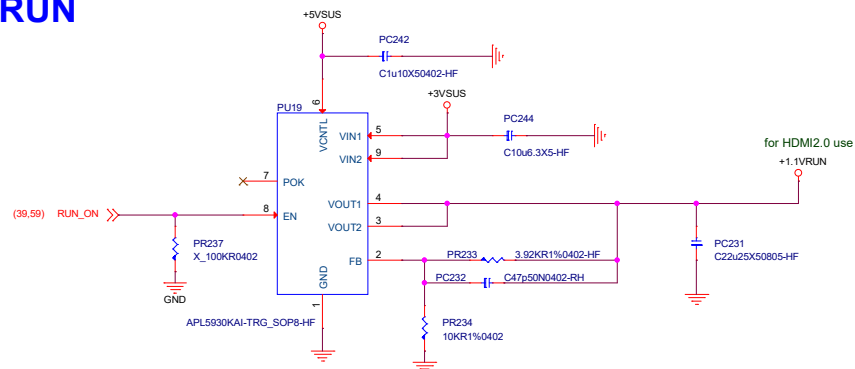
+1.05VSUS



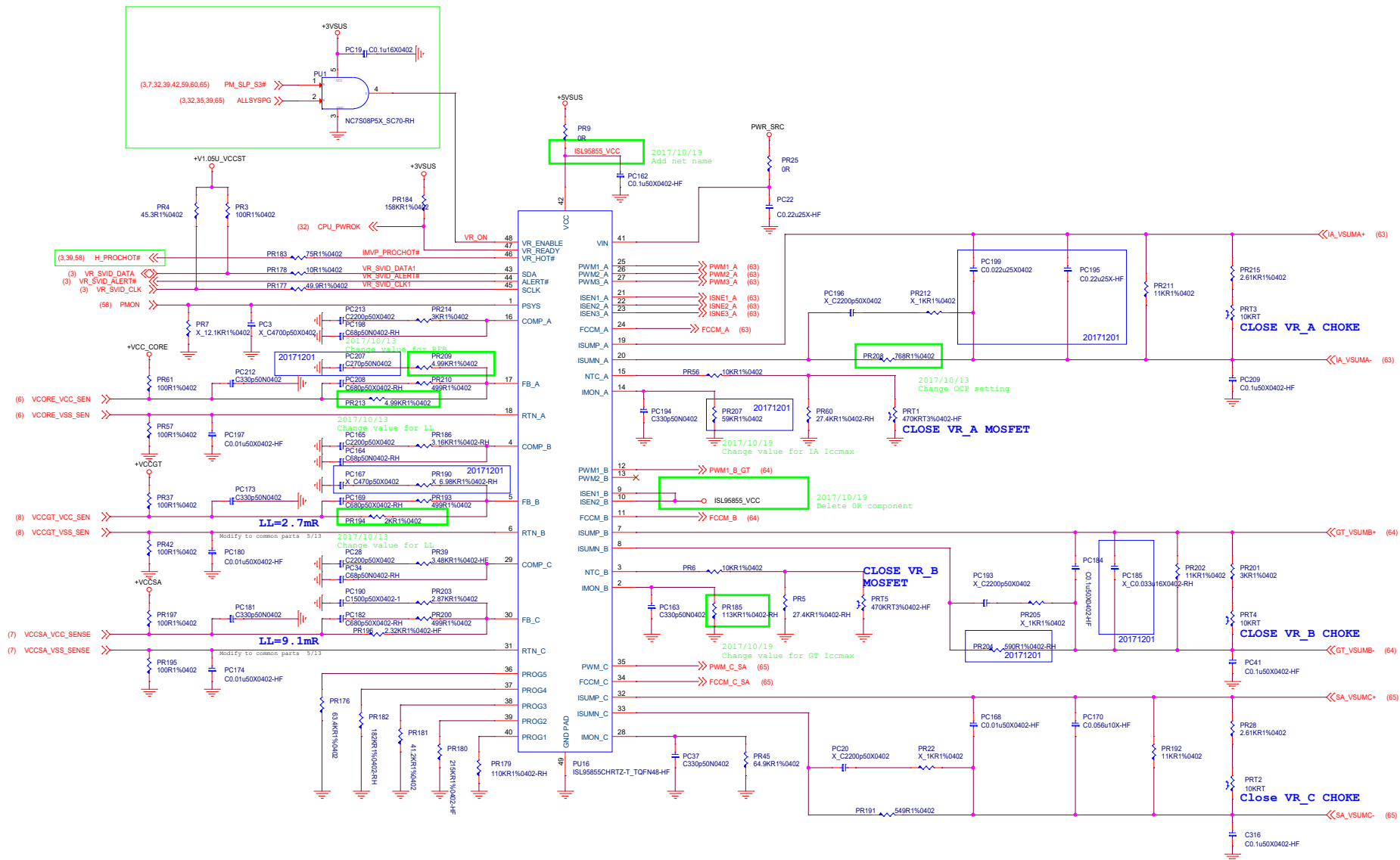
+1_8VSUS



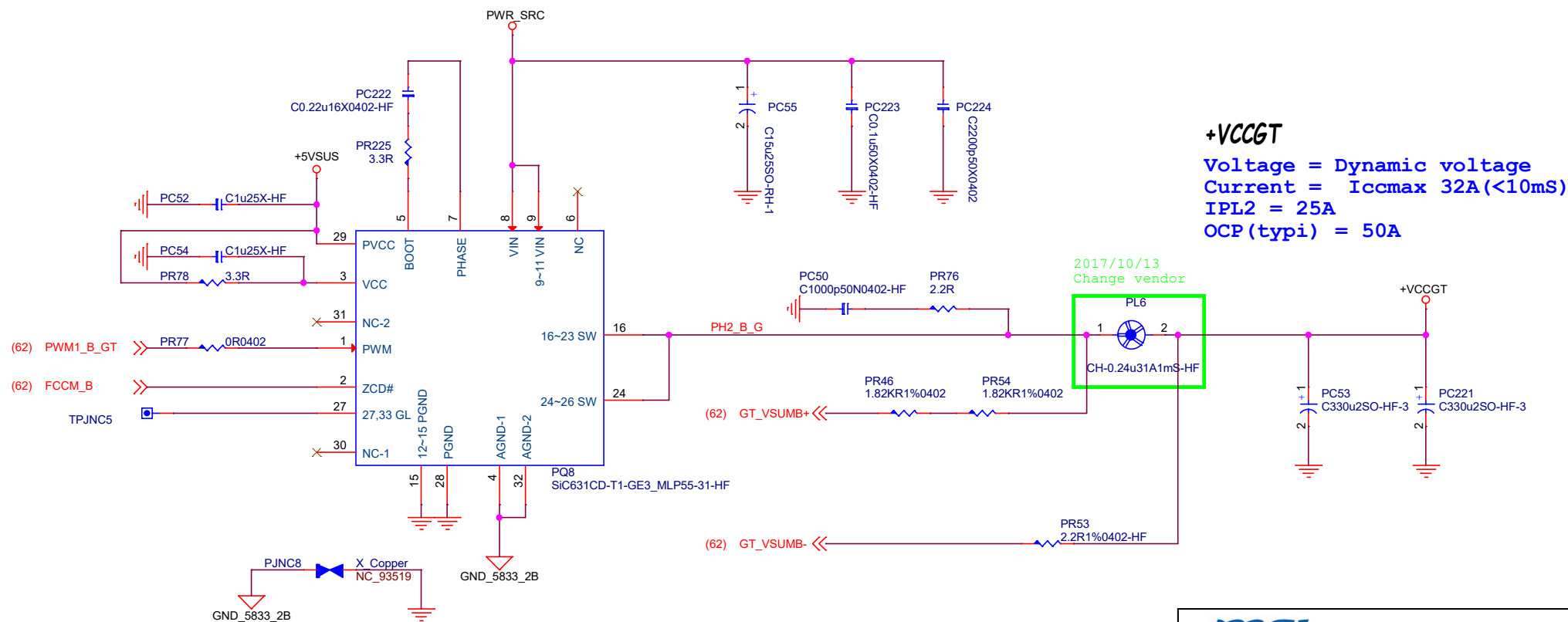
+1.1VRUN



Coffee Lake H-line
6+2 45W ISL95855C




+VCCGT

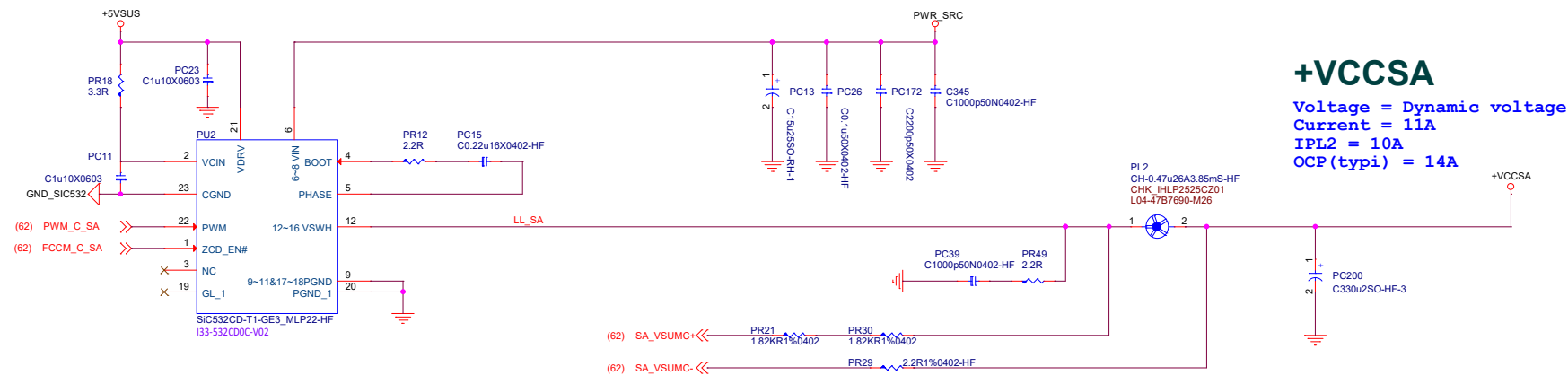


+VCCGT

Voltage = Dynamic voltage
Current = Iccmax 32A(<10mS)
IPL2 = 25A
OCP(typi) = 50A

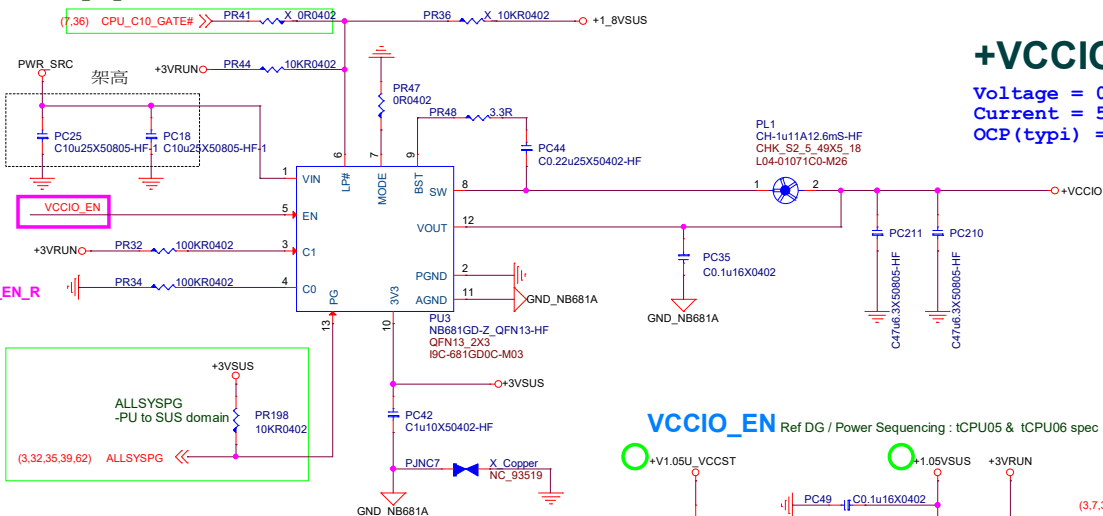
 MICRO-STAR INT'L CO.,LTD.	
Title VCCGT	
Size Custom	Document Number MS-16Q2
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+VCCSA

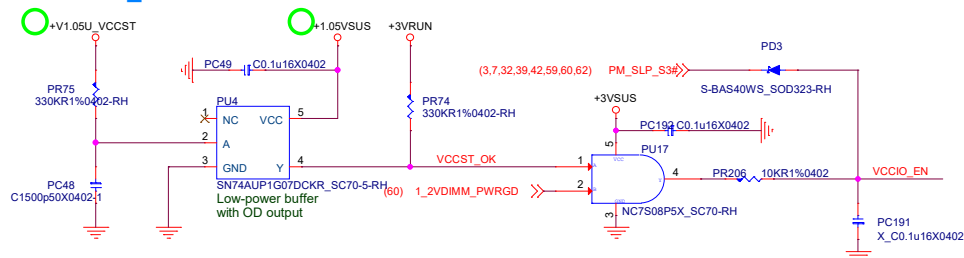


+VCCIO

Power Sequence spec tCPU27 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 240 us

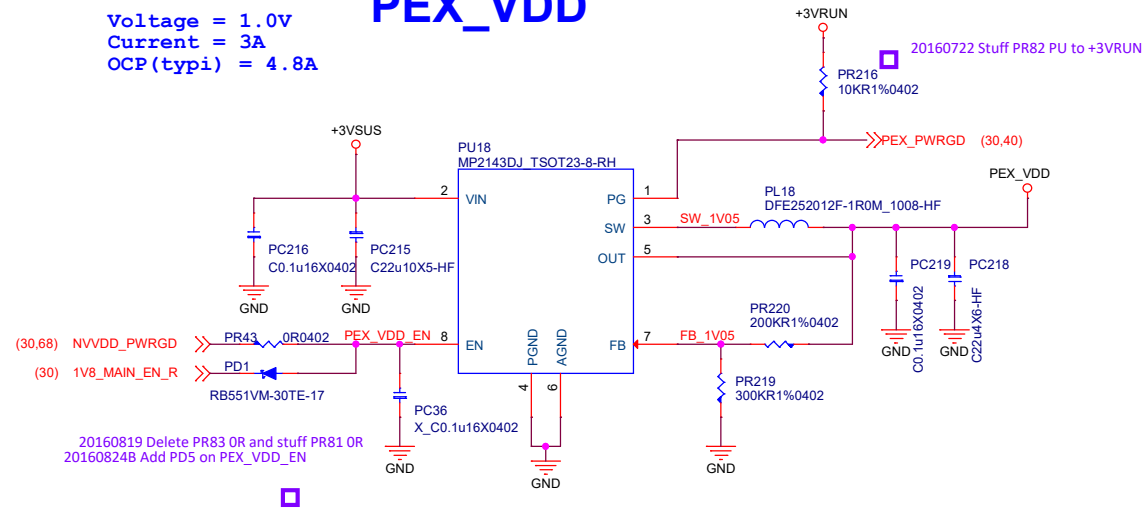


VCCIO_EN



Voltage = 1.0V
Current = 3A
OCP(typi) = 4.8A

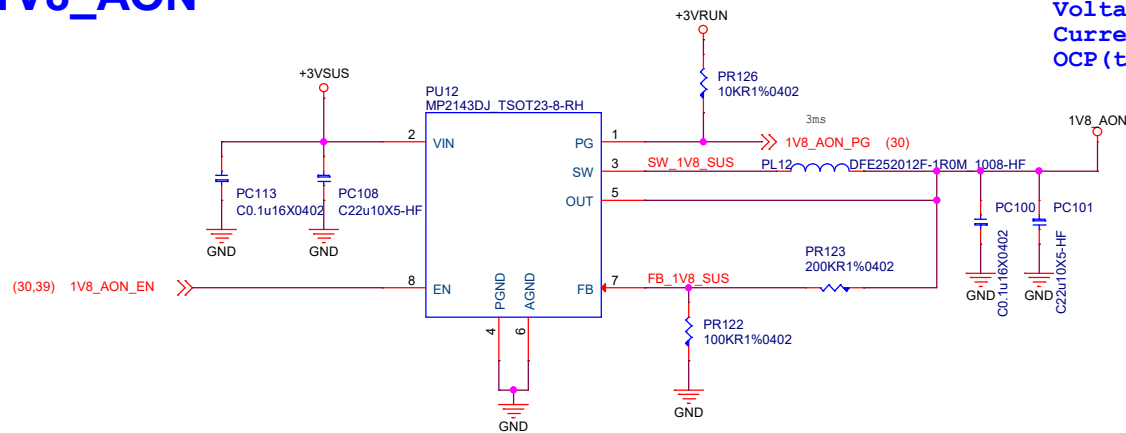
PEX_VDD



1V8_AON

1V8_AON

Voltage = 1.8V
Current = 2.26A
OCP(typi) = 4.8A



msi

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Title

1V8_AON/PEX_VDD

Size

Document Number

MS-16Q2

Rev

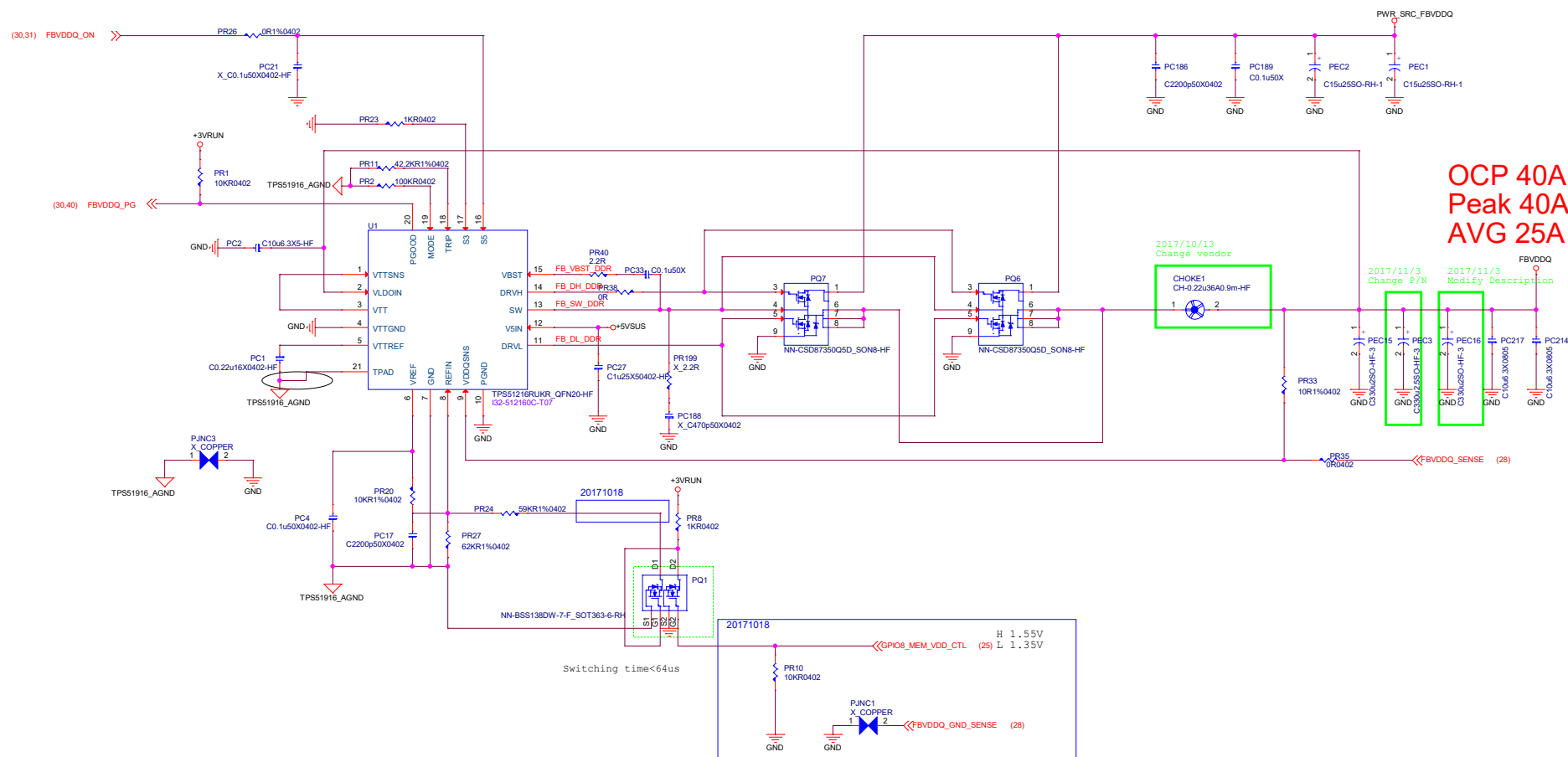
10

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OCP 40A
Peak 40A
AVG 25A

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DGPU POWER / UP9509P

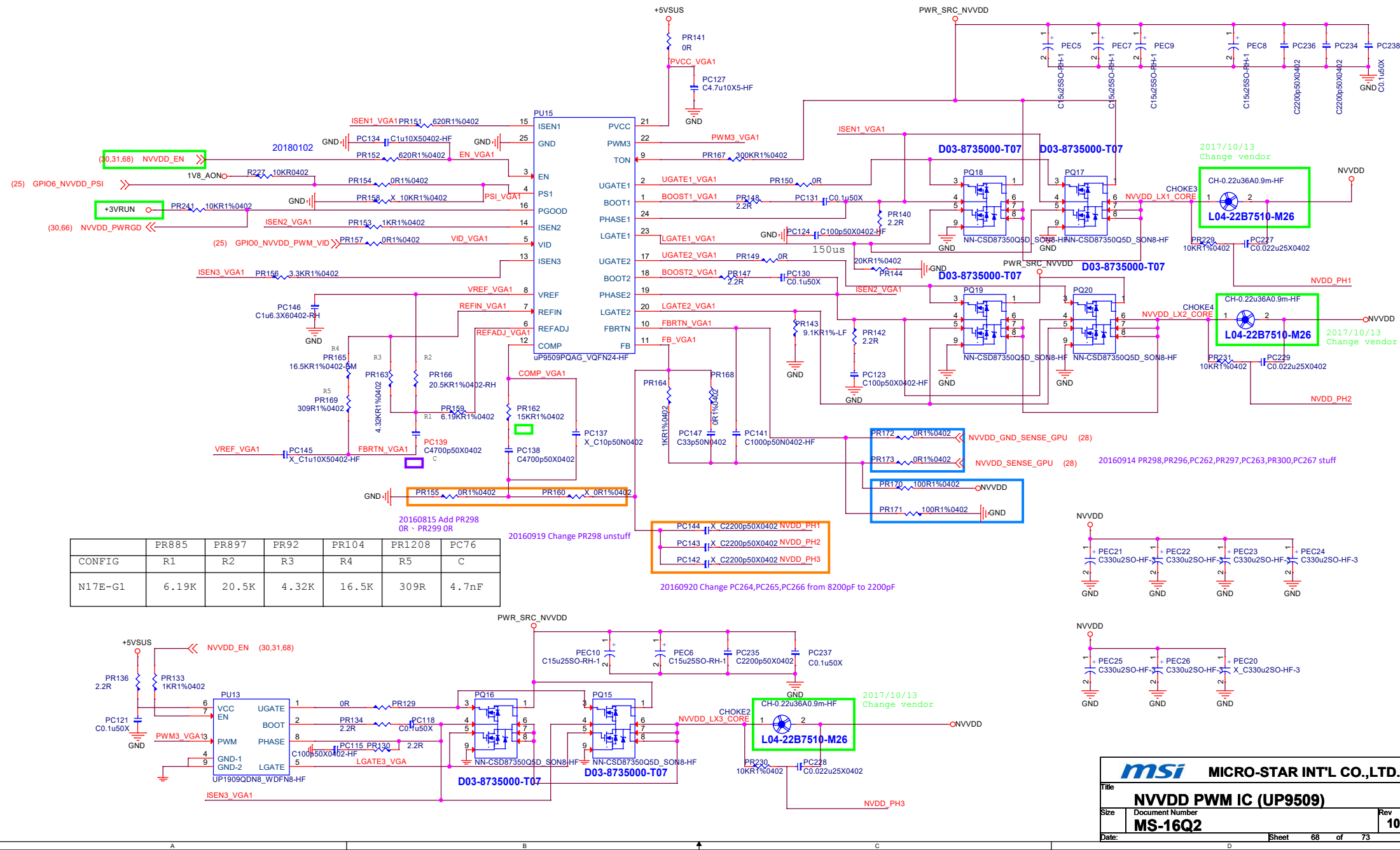
EDP-Peak 180A

EDP-Con 80A

DGPU POWER NVVDD

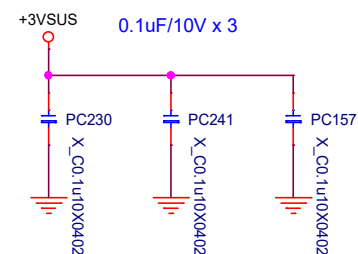
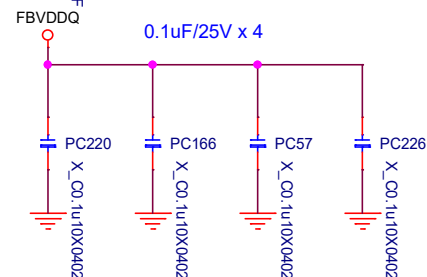
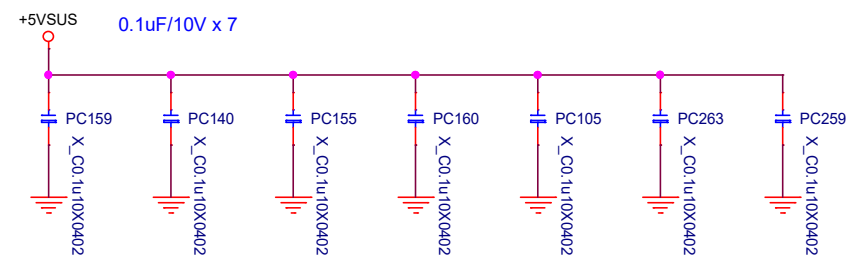
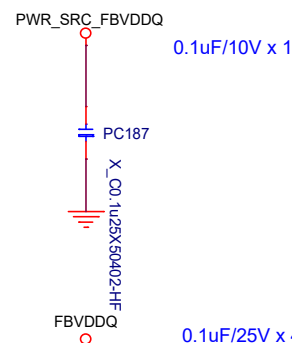
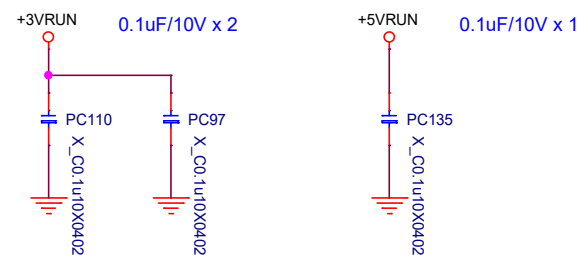
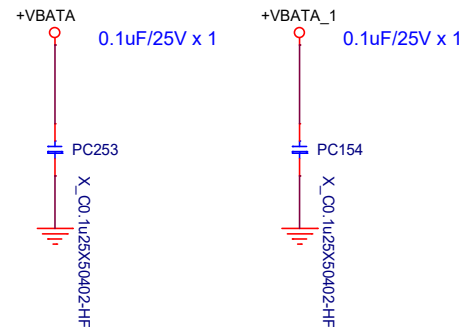
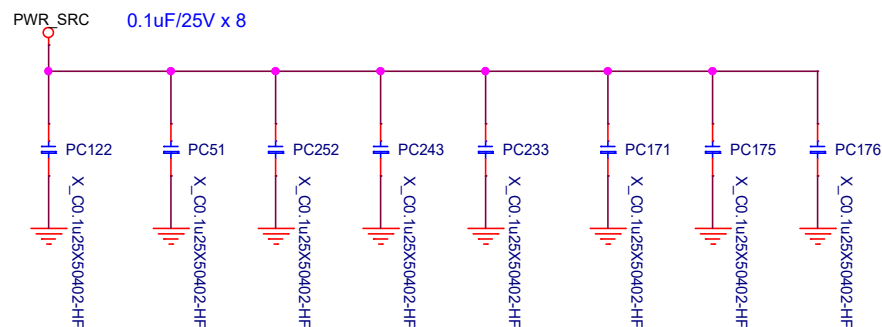
VBoot:0.8V


Vmin:0.3V / Vmax:1.3V



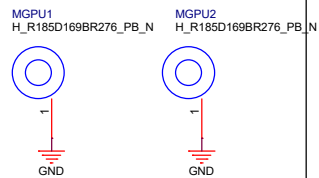
EMI

20171018

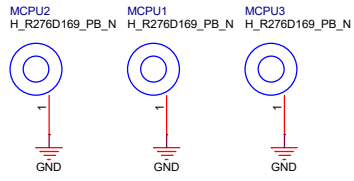


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Title			
EMI			
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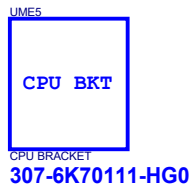
dGPU Holes



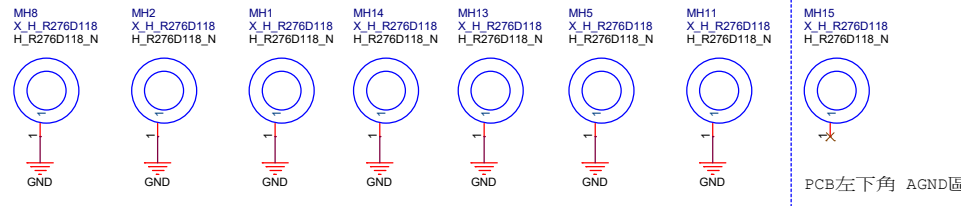
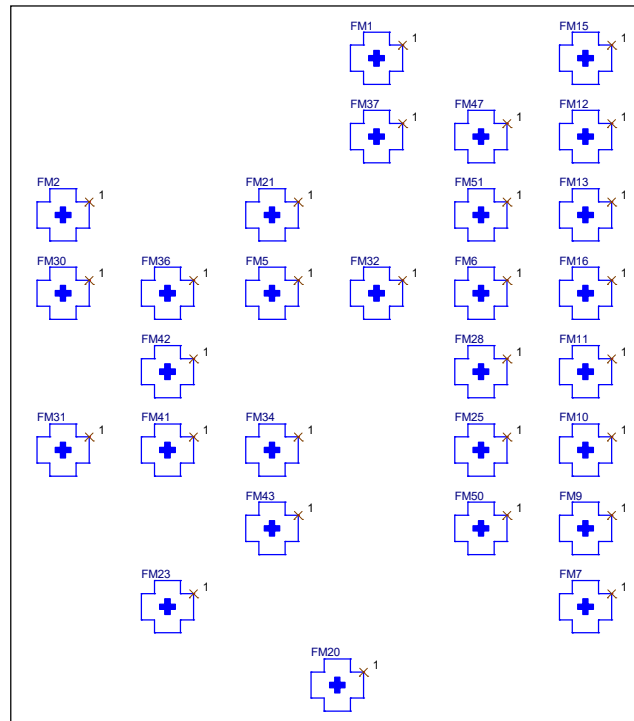
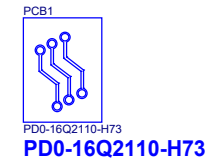
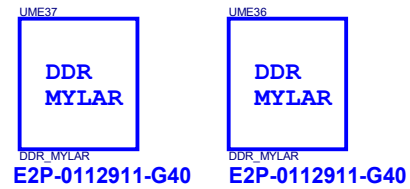
CPU Holes



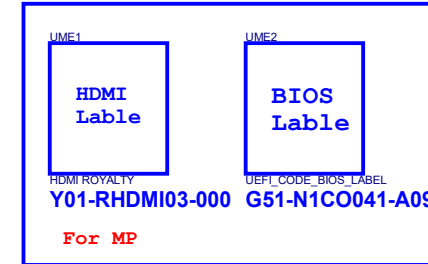
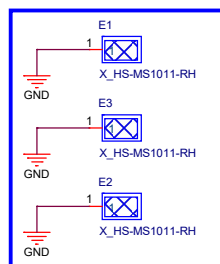
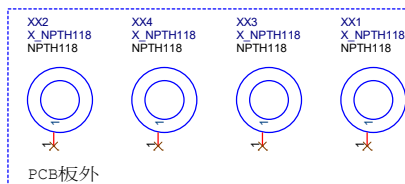
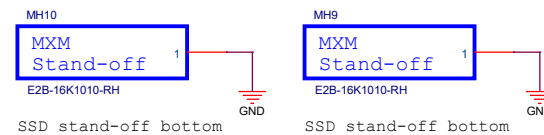
BKT



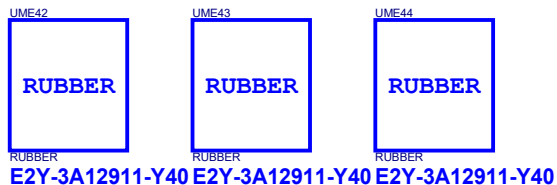
MYLAR



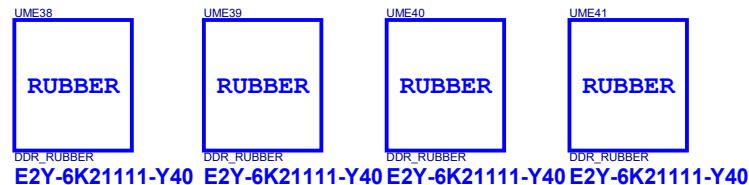
SSD Stand-off



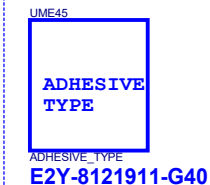
RUBBER



DDR RUBBER

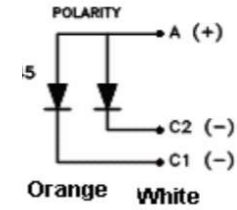
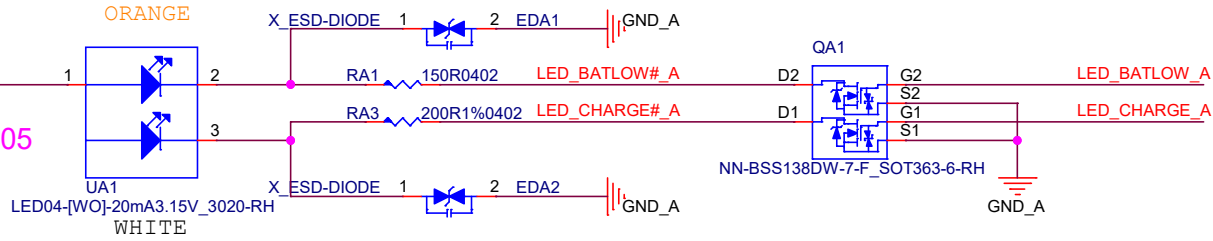


ADHESIVE_TYPE

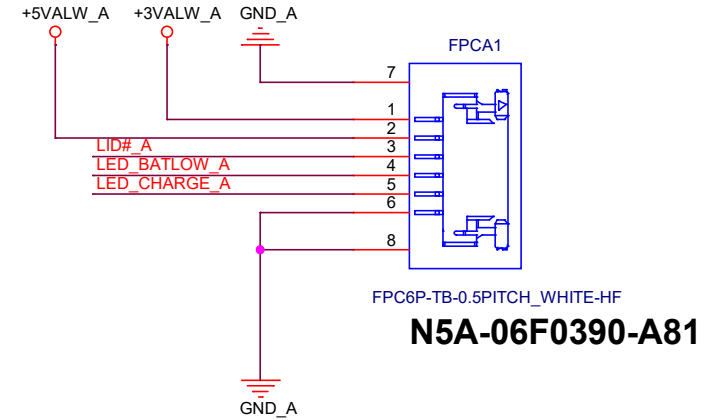
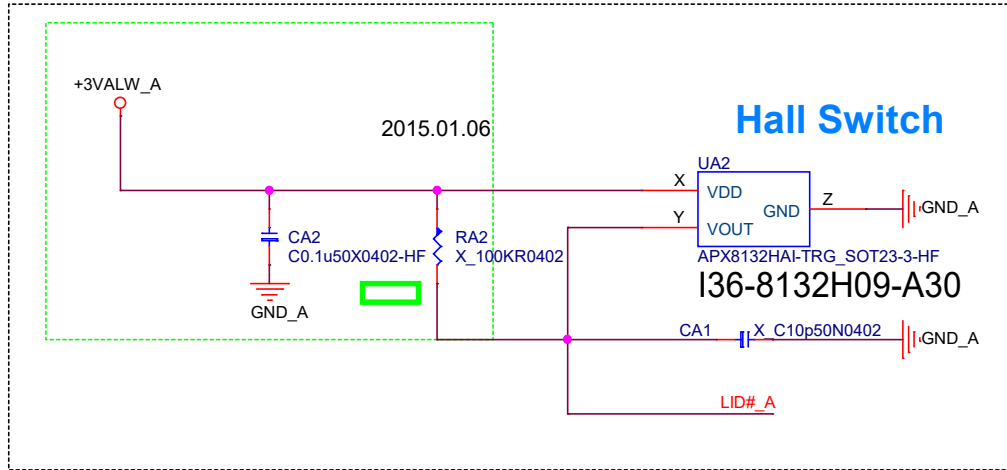


+5VALW_A

D0C-040M700-L05



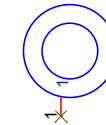
Part No.	Lens	Emitted Color	Pin Assignment
LTW-326DSKF-5A	Yellow	InGaN White	C2
		AlInGaP Orange	C1



MA1

X_NPTH_98

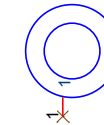
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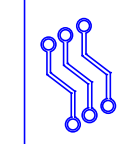
MA2

X_NPTH_98

NPTH_98




PCBA1



PD0-16Q2A10-H73

PD0-16Q2A10-H73

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LED / Hall Switch			
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Ref #543611 Chapter40
Figure 40-4. SKL-S Timing Diagram for G3 to S0/M0 (Non-Deep Sx Platform)
Table 40-5. Platform Sequencing Timing Parameters

Ref #543611 Chapter40
Figure 40-6. SKL-S Timing Diagram for S0 to G3 [Non-Deep
Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters



History

16Q2 10

DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION	DATE	PAGE	DESCRIPTION
20171005	ALL 32 58 70 56 48,50	first version from 16Q2 Unstuff R616 (PCH-LP Only) Unstuff PR30289(H_PROCHOT#) Modify ME/Screw Modify USB to N53-09M1071-AF2 Modify 22R/0201 to 22R/0402									
20171012	55 39,50 2 50 47	Unstuff R100 for CRB R10271/R10272 move to EC side for Vendor. power on block (DIMM_ON_2V5) Remove C10229 Modify U10033(ALC1220) to B05-012203C-R09									
20171016	48 22 26 24 22 45 56 46	Set POR1 to High for Vendor. 1V8_MAIN add C10865(1uF/0402) for Nvidia check. VID_PLLVDD add C10866(4.7uF/0402) for Nvidia check. PEX_VDD add C10867(1uF/0402) for Nvidia check. 1V8_MAIN add C10868(0.1uF/0402) & C10869(4.7uF/0402) for Nvidia check. NVVDD add PEC30005(330uF) for Nvidia check. FPC PIN Swap for FP Con. Modify ESD for USB3.1 Layout. Remover R10566/R10570 for Layout.									
20171017	41 40	EL10007 pin swap for Layout. Add PEX_PWRGD for Nvidia check.									
20171018	67 69	Remove R/C for Power Add EMI Cap for EMI									
20171019	69 56	Modify EMI Cap for EMI Modify power circuit for power . Add 10uF/0402 for Vendor .									
20171020	63 41	Remove PC151 for Power Add C30320 for EMI									
20171023	All	Rename									
20171024	All	Rename Con.									
20171025	All	ALC1220 change to B05-012204C-R09(VB2) SSC_EN pull High for Asmedia.									
20171030	All	0A BOM									
20171201	59 62 63	Unstuff PEC4 Stuff PEC14 Modify PC195 to C11-2242633-W08(0.22uF) Modify PC199 to C11-2232032-W08(0.022uF) Unstuff PC185, PC167, PR190 Modify PC207 to C11-2711022-W08(270pF) Modify PR207 to R11-0593T12-W08(59K-ohm) Modify PR204 to R11-0591T12-W08(590-ohm) Unstuff PC206 Stuff PC203									
20171204	All 48 9,10 45 9,10 62 32 47 32	Modify D03-65D8L09-D07 to D03-138DW19-D07 (PQ1,PQ2,PQ23,PQ29,PQ34,Q2,Q8,Q34,Q35,Q36,Q38,Q40,Q43,Q46,Q63,QA1) Stuff R646 , unstuff R650 for Audio Vendor. Modify C982,C1008 to C71-331037E-P01 for ME Unstuff SW1 for ME Stuff C946,C1036 for SA Modify PR184 to R11-1583T12-W08 for Sequence Modify C132 to C11-1057412-Y01 for Sequence Modify C1219,C1220 to C11-2267313-M09 for Audio Remove BAT2									
20171207	32 66	Stuff R122 for Sequence Unstuff R128 for Sequence Modify PD1 to D01-RB55120-R06									
20180102	40 49 68	Stuff R199 Stuff R188 , unstuff R189 Stuff PC134 Modify PR152 to R11-0621T12-W08									
20180103	 69 56 32,39 31 41 3-8 32-38	10 Swap RTC1 BAT2 change to D06-0105701-K26 Add C1245~C1248 for SA,(USB Eye) Remove EL6,EL7,R364,R365 for Asmedia. Add EC_PCHPWROK for power sequence. Modify PC132,PC136,PC148,PC149 to C11-1067620-M09(0805). Add R690(100K) for Panel Flicker issue. Modify U4(CPU) to OAD-16K5004-I06(QS I7-8750H). Modify U13(PCH) to OB1-16K5002-I06 (HM370(QNWF)).									
20180104	60	PJNC9 Change to NC_93519 for layout									
20180111	34 34,46 46	PCIE17-20 Change to PCIE21-24 Remove M2_SSD2_PDET Swap PCIE2_M2_RX17N & PCIE2_M2_RX17P									
20180111	70,71 71 47 70	PCB Ver. 1.0 RA3 Change to R11-0201T12-W08(200 ohm) Stuff C237 Add RUBBER*3 (E2Y-3A12911-Y40) for ME Add DDR_RUBBER*4 (E2Y-6K21111-Y40) for ME Add ADHESIVE_TYPE*1 (E2Y-8121911-G40) for ME									
20180125	42	U28 Change to B07-L634015-I06									